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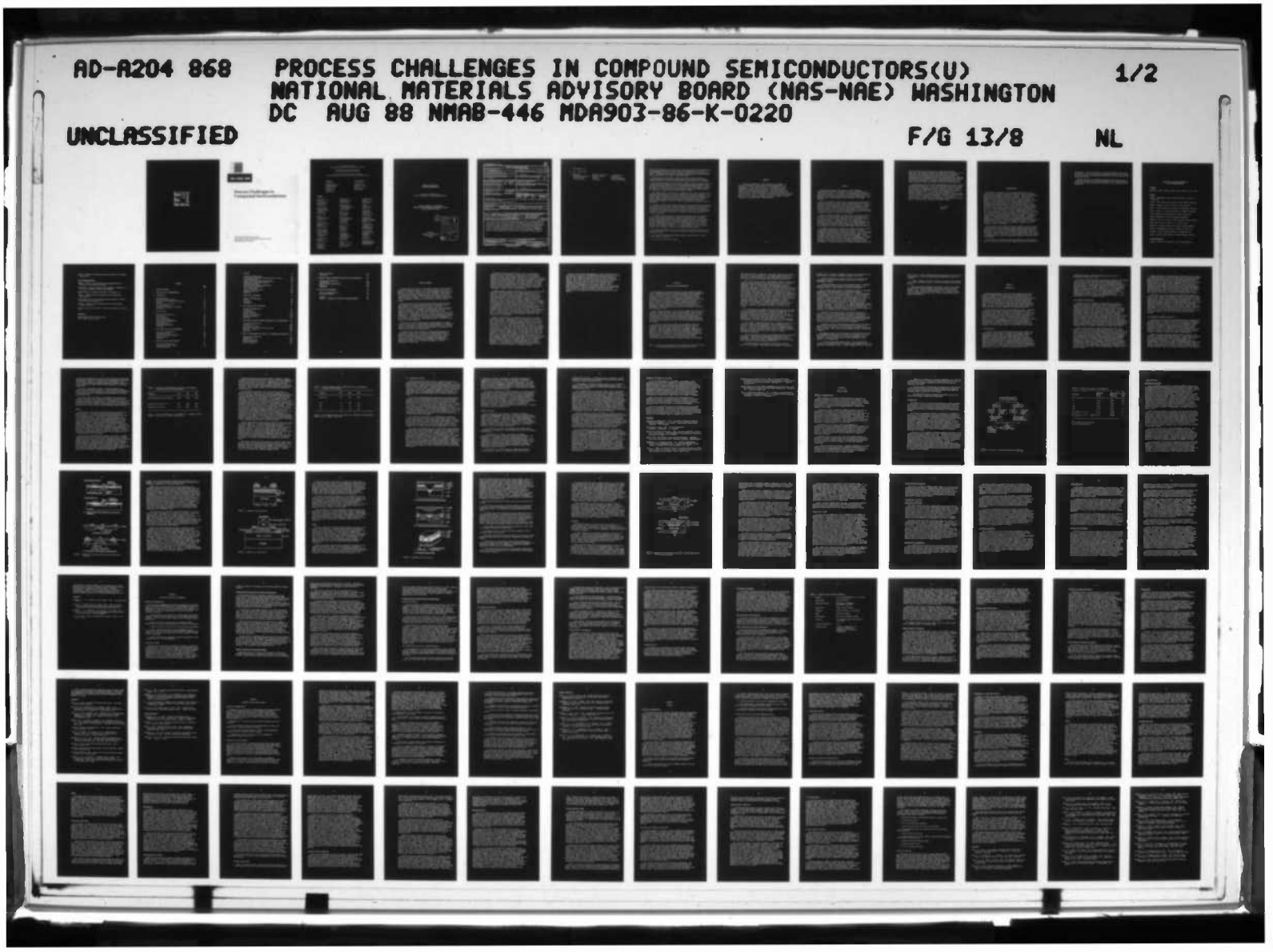

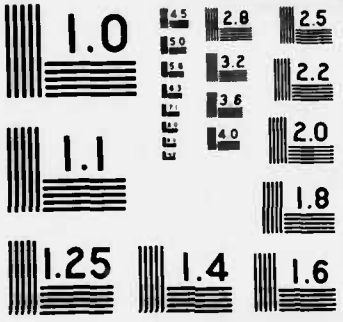
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8/88

PROCESS CHALLENGES IN COMPOUND SEMICONDUCTORS

Report of the Committee on
Process Challenges in Compound Semiconductors

NATIONAL MATERIALS ADVISORY BOARD
COMMISSION ON ENGINEERING AND TECHNICAL SYSTEMS
NATIONAL RESEARCH COUNCIL

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Compound semiconductors, such as GaAs, InP, and HgCdTe, are essential components in future photonics and microelectronics technologies. If the United States is to be competitive in these technologies, attention must be directed to the reproducible and affordable processing of these materials. This report assesses the current status of compound semiconductor processing technology and identifies factors that limit the ability to fabricate advanced electronic and optoelectronic devices. Emphasis is placed on current and near-term devices, but the process technologies discussed are generic to future components and systems based on these materials. Keywords;

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NOTICE: The project that is the subject of this report was approved by the Governing Board of the National Research Council, whose members are drawn from the councils of the National Academy of Sciences, the National Academy of Engineering, and the Institute of Medicine. The members of the committee responsible for the report were chosen for their special competences and with regard for appropriate balance.

This report has been reviewed by a group other than the authors according to procedures approved by a Report Review Committee consisting of members of the National Academy of Sciences, the National Academy of Engineering, and the Institute of Medicine.

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ABSTRACT

Compound semiconductors, such as GaAs, InP, and HgCdTe, are essential components in future photonics and microelectronics technologies. If the United States is to be competitive in these technologies, attention must be directed to the reproducible and affordable processing of these materials. This report assesses the current status of compound semiconductor processing technology and identifies factors that limit the ability to fabricate advanced electronic and optoelectronic devices. Emphasis is placed on current and near-term devices, but the process technologies discussed are generic to future components and systems based on these materials.

PREFACE

Compound semiconductors offer properties and performance characteristics not readily available in silicon, the mainstay of the semiconductor industry. In particular, the development and production of optoelectronic devices and ultrahigh-speed and high-frequency devices depend on compound semiconductors such as gallium arsenide (GaAs), indium phosphide (InP), mercury cadmium telluride (HgCdTe), and related compounds.

There is considerable interest today in advancing the technology for producing these materials, and extensive dedicated effort is directed to this end by industry, government, and university laboratories. Complex structures for new applications require special processing and process control procedures. These are the limiting factors that need to be overcome, particularly in an industrial environment, if the United States is to fully realize the potential for improved technology and to maintain a competitive position in future high technology.

Specific processes sometimes are applicable to a particular material, so discussion of some processes often may involve that material only. This report is heavily biased toward GaAs and its processing because of the wide attention it is receiving today as a next-generation semiconductor material. Needless to say, other compound semiconductor materials also have important applications (e.g., InP and HgCdTe). They are addressed to show where similar problems and limitations exist in their preparation and which processing steps differ from those for GaAs.

The committee members from industry and academia represented a balance of knowledge and experience in chemistry, electronics, electrical engineering, process modeling, and materials science. In areas where gaps in members' backgrounds and experience were evident, experts outside of the committee were invited to give presentations and supply written documents on specialized topics of concern to the committee. (The guests and their areas of discussion are listed in the Acknowledgments.) This permitted the committee to fulfill its charge, which was to make an assessment of the state of the art of processing, including foreign developments in compound semiconductors; provide a discussion of new and

novel processing techniques applicable to compound semiconductor preparation; identify the of factors that today limit the effective use of these processing techniques; examine the applicability of modeling techniques to the understanding and control of processing steps, with possible prediction of materials, device, and circuit properties; and make recommendations for R&D efforts aimed at understanding the processing that could lead to improvement or elimination of existing deficiencies that limit the ability to fabricate complex structures with these materials.

This examination deals heavily with processing and the eventual control of crucial processing steps. To this end, the committee strives to direct the attention of research and production personnel, in both the military and the commercial communities, to where a concerted effort is needed to advance the present state of the art that will increase device yield and decrease production costs. The committee feels strongly that the commercial community, in particular, must be involved as a major performer in this program; but government leadership is essential to provide funding incentives and to coordinate the development of a technology base. Industry awareness of the contents of this report is essential to properly direct current and future commercial development efforts.

A. M. Glass
Chairman

ACKNOWLEDGMENTS

The committee is grateful to the following individuals for their presentations to the committee and their submission of written documents for use by the committee in preparing its report: James M. Ballingall, of General Electric Company's Electronics Laboratory, who discussed commercial needs in molecular beam epitaxy; Clive A. Collins, of IBM Corporation, who discussed the role of GaAs in high-end computers; Robert Dutton, of Stanford University, who discussed modeling devices and processes; Jai K. Hakhu, of Rockwell International Corpcration, who discussed how past developments in silicon technology relate to future GaAs production; William G. Howard, of Motorola, who discussed economic analysis of compound semiconductors; Kheldun R. Kahn, of BIS Mackintosh Ltd. (U.K.), who discussed market trends in compound semiconductors; Conilee G. Kirkpatrick, formerly of Rockwell International Corporation, who discussed GaAs pilot-line status and problems; Mike Malbon, of AVANTEK Inc., who discussed processing challenges in III-V process controls; Tsuneo Nakahara, of Sumitomo Electric Industries (Japan), who discussed the future of compound semiconductors in Japan; Norman E. Schumaker, of EMCORE Inc., who discussed metallo-organic chemical vapor deposition equipment; Gary Troeger, of McDonnell Douglas Microelectronics Center, who discussed GaAs pilot-line status and problems; and Robert K. Willardson, formerly of Cryscon Technologies, who discussed a supplier's view of substrates, needs, and feedback.

The government liaison representatives are thanked for participating in committee discussions and providing valuable support materials and data for committee use. They were most helpful in assisting the committee in defining the scope of the study and offering needed guidance during the development of the committee's report drafts. Special thanks go to Julian G. Blake and Harvey C. Nathanson, who, as technical advisors, made notable contributions to the report and assisted the committee in various areas of its assessment.

The chairman of the committee thanks the members for their dedication and for the patience shown during the numerous iterations and revisions of

report drafts. Particular thanks go to the committee members who served as chapter or section coordinators to assemble pertinent facts for various parts of the report and who presented the data in a timely open-minded and professional manner.

Finally, the committee gratefully acknowledges the untiring support of Dr. George Economos, the senior program officer of the National Materials Advisory Board, and his secretary, Ms. Aida Neel, in all stages of report preparation.

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EXECUTIVE SUMMARY

The rapid decline of the U.S. semiconductor industry in global markets has received national attention. In an attempt to halt this decline, a number of collaborative initiatives have been established that combine the resources of industry, universities, and the government. These include the Semiconductor Research Corporation (SRC), the Microelectronics and Computer Corporation (MCC), and the Semiconductor Industries Association consortium known as SEMATECH. All of these major initiatives address only silicon technology, a technology with substantial existing commercial markets.

The next generation of advanced microelectronics and optoelectronics technology will use compound semiconductors such as gallium arsenide, indium phosphide, and mercury cadmium telluride. For these semiconductors, the current markets are small and are driven primarily by military requirements; the manufacturing technologies are only in early stages of development. Yet compound semiconductors have unique capabilities, not achievable with silicon, that will be vital for the next generation of ultrahigh-speed computers, microwave generation, and optical communication. Integrated optoelectronic devices for high-speed switching and information processing are now emerging from research laboratories, but the processing science and technologies necessary to manufacture such devices are in their infancy.

To avoid loss of these technologies to overseas competitors, proper attention must be given to these advanced technologies now. A coordinated national strategy must be formulated that makes the best use of existing resources to establish the technology base necessary to capitalize on the opportunities presented by these materials.

The Committee on Process Challenges in Compound Semiconductors was established to examine the current status of compound semiconductor processing technology and to identify factors that currently limit the ability to fabricate advanced electronic and optoelectronic devices. These factors include limitations in fundamental understanding of materials and processes, and processing equipment. In addition, the committee was asked to make a comparative assessment of foreign developments in this field.

Processing of compound semiconductors is not a straightforward extension of silicon technology. Factors such as lattice mismatch, surface passivation, vapor pressure differences of the constituent elements, and stoichiometric defects all add to the complexity of material preparation and device fabrication. Opportunities presented by composite, artificially-structured materials, which permit the design of specific optical and electronic properties, need special attention. The report addresses only those issues specific to compound semiconductors that cannot be directly transferred from silicon technology. These include issues such as substrate growth and preparation, epitaxy, etching, lithography, dielectric films, and metallization.

It became evident during this examination that a major obstacle to the affordable, high-yield manufacture of compound semiconductors is the serious lack of understanding of relationships among the materials properties, the various processing parameters, and the eventual device yield and performance. Improved understanding requires coordinated interdisciplinary research ard development, including disciplines of chemistry, physics, surface science, chemical, mechanical and electrical engineering, together with parallel theoretical modeling of the equipment and processes used in compound semiconductor device production. A number of uncoordinated subcritical research and development efforts are currently funded in the United States that have overlapping programs and are generally not close enough to the device manufacturing line to optimize process technology for improving device yield. The throughput of commercial device lines is often too small to establish proper process control. Communication of processing technology between R&D centers is poor. A better coordination of these programs is essential to the advancement of the technology.

Because of these factors, the committee believes that the federal government must play a leadership role in partnership with the private sector and academia. Although defense needs currently account for the major market share of U.S. compound semiconductor materials and devices, the potential exists for large commercial markets in the future. The fabrication of low cost, high yield, high stability devices and circuits is an essential prerequisite to expanding commercial markets for compound semiconductors. In the nearer term (within 5 years), these markets will include high speed electronic circuits for computations and information processing, satellite communications, and wide bandwidth circuits, also components for optical communications. In the longer term (5 years and beyond), it is anticipated that photonic and electronic devices will become mutually compatible components of integrated optoelectronic systems for ultrahigh throughput information processing. Just as the growth of high technology over the last two decades has been closely linked to advances in silicon materials processing technology, so will future progress be closely dependent on compound semiconductor processing technology. A long-term focused U.S. commitment to this technology is required to avoid total dependence on overseas technology.

Research and development coordination and close coupling feedback of the materials research with the processing and device communities are the most important components in helping correct the domestic industry's decline. This includes coordinating the activities of the university research centers with those of the government and industrial centers. In addition, focus of the research effort must be directed toward a commercial technology base, since this is the essential link for establishing and maintaining a viable defense industrial base. Administering and staffing of new technology centers is an area needing further assessment; a MITI-style approach of sharing staff between such centers has not been tested in the United States and, with some modifications, this approach may find productive application in these centers.

CHAPTER 1

CONCLUSIONS AND RECOMMENDATIONS

The advantages of compound semiconductors, such as gallium arsenide (GaAs), indium phosphide (InP), and mercury cadmium telluride (HgCdTe) for use in optoelectronic devices and in ultrahigh-speed or high-freqency electronic devices, are well established. In these areas, compound semiconductor devices provide unique performance enhancements over the capabilities of silicon devices. Components based on these materials will be vital elements in commercial and military electronic systems. Realization of the enhanced performance of compound semiconductors has, however, been greatly hampered by difficulties in developing the appropriate process technology base to achieve the high yield, high performance, and high reliability necessary for these materials to take a place alongside silicon.

Major research advances in recent years have demonstrated new physical phenomena, improved materials, and new device concepts. Many of these involve the fabrication of multilayer structures for quantum well lasers and detectors, high-electron-mobility devices, and nonlinear optical switching devices. Equipment has been developed for the fabrication of such exploratory devices, but these are generally customized instruments for the research laboratory and are not well suited to the manufacturing environment.

In contrast to the dramatic progress in the research arena, the development of the process-technology base has been slow, and thus commercial exploitation of the science base is lagging. There is currently little firm understanding of the relationships among material parameters, process parameters, and device performance. Consequently, there is little standardization of procedures for fabricating even the simplest devices, including the initial step of substrate specification and certification. The size of the current market for compound semiconductor devices, particularly electronic devices, is not sufficiently attractive to sustain the necessary large-scale investment

NOTE: A Glossary is appended at the end of this report that explains many of the acronyms and abbreviations contained in the text.

and development efforts--especially in the small companies that dominate this field. Unless the present U.S. government support structure is modified, the committee does not see any significant near-term prospects for closing the ever-widening gap between research and manufacture.

This is not the case in Japan. The Japanese electronics industry has targeted compound semiconductor technology with the intent of gaining a large market share of future products and systems that use this technology. This is a long-term goal, with government-coordinated research and development that began in the late 1970s and was not tied to short-term deliverables. Japan increased its share of world silicon-based semiconductor markets from a small fraction 10 years ago to over 50 percent today. The fraction is estimated to be greater than 75 percent in the new compound semiconductor-based markets. Because of its emphasis on manufacturing technology, Japan is better poised than the United States to take advantage of new market developments, as they did a few years ago in the case of GaAs lasers for compact disk recorders and InGaAsP lasers for lightwave communication. Current Japanese dominance in compound semiconductor technology will contribute substantially to Japan's dominance of high-technology telecommunications and computer systems of the future. If corrective action is not taken, the equivalent U.S. materials, components, and systems businesses will not grow or even survive.

It is imperative that programs be directed toward advancing the state of the art of compound semiconductor processing technology and attaining the proper degree of process control necessary to reliably and reproducibly manufacture structures on a commercial scale. Processes developed for one compound semiconductor such as GaAs are often directly applicable to others--InP, InGaAs, and CdTe--with only minor modifications. Furthermore, processes developed for current technology are prerequisites for the more complex device structures of the future.

In this report, recommendations specific to individual processes are listed at the beginning of each chapter. These recommendations are directed to industrial R&D management as well as to government funding agencies. However, the following general technical recommendations set forth by the committee represent a first priority to achieve an effective technology and competitive international position in compound semiconductor manufacture:

- Establish programs to clarify the relationships between the crystal growth and subsequent processing procedures and the device yield and performance. Close interaction and feedback between each step of semiconductor fabrication is vital to understanding how each processing step is affected by the preceding process history.

- Establish detailed specifications for individual materials, processes, and equipment. This includes specifications for substrates,

epitaxial layers, etchants, lithographic processes, ion implantation, and metallization, as outlined in individual chapters that follow.

- Develop equipment and processes suitable for the manufacturing environment for the low-cost, high-yield fabrication of compound semiconductor devices.

- Develop techniques for in situ and in-process control. This must include intelligent control systems and theoretical modeling of the processes as well as a broad range of experimental diagnostics.

These technical issues require the integration of efforts of equipment manufacturers, materials suppliers, research and development organizations, and semiconductor fabrication lines. While market forces drive development of 1- to 2-year deliverables, 2- to 5-year development is not adequately supported, either by the private sector or by the government. Long-term commitment to product development is essential for success. Government incentives are particularly appropriate, since defense needs today account for the major market share of GaAs and virtually all II-VI materials and devices. Significantly greater coordination among U.S. participants in the compound semiconductor area is strongly recommended. In this respect, the federal government must play a leadership role but in partnership with private-sector industry and academia. The committee therefore believes that the following actions are appropriate to optimize the use of national resources:

- Establish a prestigious national review panel consisting of industrial, university, and government engineers and scientists to (a) develop a national compound semiconductor strategy, (b) coordinate activities and funding, and (c) make appropriate recommendations for R&D. The present procedure of overlapping programs, often poorly coordinated and too often tied to narrow and short-term interests of specific industries or government agencies, should be eliminated.

- Establish critically funded technology centers with joint industry and university participation. Successful operation of such centers depends heavily on the selection and coordination of projects and on the level of funding. This, in turn, will influence the level of industrial commitment.

The committee endorses the 1987 proposal of the Defense Science Board and IEEE/DARPA Strategic Materials Initiative for centers of this kind. Such centers for the expansion of the national technology base are analogous to existing national centers for the advancement of basic science. It is proposed that

- University engineering research centers, such as the NSF-ERC programs, be coordinated with the technology centers suggested earlier and with existing DOD ManTech centers. Academic programs at the B.S. level as

well as the Ph.D. level in materials processing and manufacturing sciences are necessary to increase the availability of appropriately qualified students.

- Greater emphasis be placed on using the existing government-funded pilot lines as a national facility to solve the technical issues outlined earlier.

Industry-government partnership is essential. Military requirements often are aimed at high-performance specialized products with little regard for cost. The United States cannot sustain a vigorous defense industry without a healthy commercial industry. It is therefore vital that future emphasis be placed on cost, yield, and manufacturability of compound semiconductors.

CHAPTER 2

INTRODUCTION

Compound semiconductors will be essential elements in electronics areas of ultrahigh-frequency computation, microwave generation, and optical transmission. The future potential of novel structures for integrated optoelectronic devices for high-speed switching and information processing has just begun to be realized in the research laboratory. Unless substantial changes occur very soon in the way products are identified and brought from the research laboratory to the marketplace, control of these technologies is destined to move offshore during the 1990s. The loss of this critical technology will adversely affect U.S. competitiveness in avionics, computers, and information systems.

Current commercial markets for these products are small. Leadership by the federal government is required for developing the necessary technology base to produce high-yield, low-cost devices. In this report, the committee makes a critical assessment of compound semiconductor processing technology and identifies technical factors that limit our ability to manufacture low-cost, high-yield devices and circuits. In addition, the committee proposes a "recovery" plan of cooperative research that includes (a) the establishment of a national review panel to coordinate R&D in compound semiconductors, (b) the establishment of national technology centers, and (c) the establishment of university engineering centers to train students at all levels in this key area.

STUDY MOTIVATION

A number of reports have been published recently that address the status of U.S. microelectronics research and development [Office of Technology Assessment, 1986], the competitive position of the U.S. semiconductor industry [National Materials Advisory Board, 1986; Federation of Materials Societies, 1986; JTECH, 1985], the impact of cooperative research in Japan on its microelectronics industry [Merz, 1986], a possible approach to cooperative research in the United States [McLoughlin and Miller, 1987], the benefits and risks associated with federal funding of a consortium of electronics industries [Congressional Budget Office, 1987], and an examination of the roles that the National Laboratories may play to reverse the current decline of the U.S.

semiconductor industry [National Materials Advisory Board and Manufacturing Studies Board, 1987].

This report differs from these others in that it addresses the current state of the art of the processing of compound semiconductors and identifies factors that limit the ability to fabricate reproducible, low-cost devices. It also assesses the present scientific status of U.S. and foreign compound semiconductor materials and the processes used to fabricate devices. It is evident, however, that, to make significant advances in compound semiconductor technology, it is not sufficient to identify deficiencies in U.S. scientific knowledge and technical capabilites; it is also necessary to consider improvements in the way research and development is done. The committee makes some recommendations on future research and development as well as on how to make better use of U.S. national resources.

WHY COMPOUND SEMICONDUCTORS?

Current electronics technology is dominated by the elemental semiconductor, silicon. However, with the ever-increasing need for devices with higher speeds and higher levels of integration, the limitations of entirely silicon-based electronics are becoming evident. Compound semiconductors will become increasingly important in advanced technologies because of their intrinsically higher speeds, lower power requirements, optoelectronic capabilities, and greater resistance to high-energy radiation. The higher electron velocity in compound semiconductors translates directly into greater operating frequencies and greater computation speeds using the same design rules as silicon. For high-speed computational and microwave devices, GaAs is currently the material of choice. The band structure of GaAs, InP, and related binary, ternary, and quaternary compound semiconductors permits the fabrication of efficient light-emitting structures (lasers and light-emitting diodes) of current importance for optical communication, optical interconnection of electronic chips, and consumer products such as compact disk players.

Beyond current technology, compound semiconductors offer a wide variety of new and versatile devices for future systems. By growing multilayer structures of alternating composition on the scale of a hundred angstroms (10 nm), entirely new material properties can be designed for use in optical and electronic devices. The electronic band structure of such composite materials can be tailored to meet specific requirements such as wavelength of operation or ultrahigh-speed electron transport, properties that are not attainable with an individual semiconductor. Optoelectronic circuits can be designed in which optical and electrical components are integrated on a semiconductor chip to fully capitalize on the advantages of each technology. These are areas of great potential that will evolve from current compound semiconductor technology, and they represent an exciting window on future high-performance electronic and photonic systems.

Compound semiconductor technology today is handicapped by the absence of a commercial market to provide the driving force for upgrading domestic device processing capabilities. Silicon processing technology does not generally apply to the fabrication of compound semiconductor devices. Factors that do not arise in silicon technology, such as lattice mismatch, surface passivation, vapor pressure differences of the constituent elements, and stoichiometry-related defects, in compound semiconductor technology require special crystal growth methods, processing procedures, and process control. Many of these processes need further development, and the currently limiting factors of process control must be overcome. This is particularly true in the manufacturing environment, where cost-sensitive issues such as device yield determine product viability.

Since GaAs is the most important of the compound semiconductors in terms of current market needs, emphasis is placed on that material system in this report. However, InP and InGaAsP alloys are currently of primary importance for optical communication devices, and HgCdTe alloys are the semiconductor systems of choice for infrared imaging devices. Many of the processing challenges confronting GaAs manufacture apply equally well to these other compound semiconductors. Where there are significantly different problems for different materials systems, these are addressed individually. As compound semiconductor technology advances, these newer technologies will play an increasingly important role in the total picture. At present, these other materials are much less mature in their development than GaAs, and their full potential cannot be readily assessed.

THE IMPORTANCE OF MATERIALS PROCESSING

The fabrication of compound semiconductors involves a large number of processing steps starting with the growth and preparation of substrates upon which devices and circuits are constructed. Subsequent processing steps may include the epitaxial growth of thin semiconductor layers, etching and lithography to define two-dimensional features on the semiconductor surface, ion implantation to create the appropriate electrical activity in the semiconductor, and the deposition of metallic conductors or dielectric insulators. Each of these processes must be precisely controlled to achieve reproducible characteristics.

Silicon processing technology generally cannot be applied to the fabrication of compound semiconductor devices. Factors that do not arise in silicon technology, such as lattice mismatch, surface passivation, vapor pressure differences of the constituent elements, and stoichiometry-related defects in compound semiconductor technology, require special crystal growth methods, processing procedures, and process control. However, one of the most serious issues in process control is the lack of understanding of the manner in which one processing step can influence subsequent steps and the eventual device yield. For instance,

the electrical characteristics of devices can be affected by strains and compositional uniformities that may be introduced during substrate growth and preparation, epitaxy, ion implantation, or metallization. The activity and distribution of implanted dopants are likewise influenced by stress, composition, thermal history, and the properties of dielectric encapsulants.

The cost of semiconductor devices is largely determined by the eventual yield of devices and circuits. For new devices, yields may be only a few percent. Since hundreds of devices are typically fabricated on a single wafer, material or dimensional non-uniformities can critically affect device yield.

As devices become more complex, as the number of processing steps increases, and as the size of substrates increases, precise control of each process becomes even more critical. At the present time, many of the processes need further development and the currently limiting factors of process control must be overcome. These controls are in the manufacturing environment where device yield and volume determine product availability.

MARKETS

Current markets for GaAs and growth projections into the 1990s are given in Table 2.1. The table was derived from Sumitomo Electric Industries data, and is largely consistent with data derived from other U.S. and European sources. At present, the largest market is in optoelectronic devices for communication systems and consumer markets (e.g., display and compact disk). While GaAs-based products are the largest volume markets, higher priced InP/GaAs products account for a significant fraction of the dollar amount. The worldwide market for lightwave components in 1986 was about $1 billion--about one-third being for long-haul transmission, one-half for short-haul (e.g., local area network, loop, computer network, and metropolitan area transmission), and less than 20 percent for the military. By 1992, the market in compound semiconductor optoelectronic devices is expected to increase to more than $4 billion, and lightwave systems, dependent on these devices, will be considerably greater than that figure.

The current GaAs integrated circuit market, in contrast, is largely driven by military needs. In 1985, over 75 percent of the $1.2 billion ($900 million) GaAs-IC market was military (20 percent digital, 80 percent analogue microwave). At present, most U.S. military electronics and systems companies are deeply involved in in-house efforts to demonstrate the applicability of GaAs systems by the late 1990s. Because of its ability to generate high-power, low-noise microwave signals in the 10 to 100 GHz spectrum, GaAs promises to revolutionize electronic warfare, space and terrestrial communication systems, phased array radar, commercial high-resolution television, and satellite communication.

TABLE 2.1 Worldwide Merchant Market Projections for Some Compound Semiconductor Devices ($ Million/Year)

Category	1985	1990	1995
III-V Semiconductors device total	1400	3800	8200
Electronic devices and I.C.s	300	1200	4100
Optoelectronic devices	1100	2600	4100

Source: Private communication to the committee by T. Nakahara, Sumitomo Electric Industries, Ltd. (Japan), January 1987.

Estimating the growth of the GaAs-IC market is difficult. Market research has resulted in figures of $3.8 billion in 1990 and projected to be greater than $8 billion in 1995, but extrapolations of this magnitude are inevitably subject to huge errors. Market research places the majority of this growth anticipated in digital ICs (about 50 percent of the GaAs-IC market by 1990), with the military share falling to less than 30 percent. Such projections appear to be an optimistic assessment of market parameters.

The importance of these data lies in the fact that defense is currently, and will continue to be, an important driving force of the GaAs-IC technology--much larger than the 5 percent defense-related portion of the silicon market that occurred during the 1960 to 1985 period of explosive growth in the silicon industry. Thus, a significantly higher percentage of government participation in the development of GaAs technology is required. Civilian markets for GaAs-ICs are now very small and insufficient to support the large long-term investment required for development and manufacture of GaAs-ICs. A large generic market is needed and must be created to drive the required industrial investment. The cost of a GaAs chip can be as much as 10 to 20 times that of a silicon chip. Silicon bipolar technology continues to advance, and it is not yet clear how effectively the speed advantage of GaAs devices can be used in applications such as high-end computers, where interconnection delays are as important as device delays in current circuit architectures. As architectures are modified to make use of optical interconnections, the advantages of the higher intrinsic speed of GaAs will become increasingly evident in digital systems. In the long term, it can be anticipated that photonic and electronic devices will become mutually compatible components in fully integrated optoelectronic circuits and systems.

Compound semiconductor substrate market projections from 1985 to 1995 are given in Table 2.2. The table shows that the total market is quite small and insufficient to sustain the large number of materials suppliers. Today, there are 15 U.S. companies and 11 overseas companies selling GaAs wafers. In the United States, these are mostly small companies, whereas in Japan they are large companies with a majority of the market share. Currently the largest market (about 80 percent) is for optical devices that use horizontal Bridgman-grown (HB) GaAs. Liquid-encapsulated Czochralski-grown (LEC) GaAs accounts for only about 25 percent of the current GaAs market, but the growth of the market for LEC material is expected to expand much more rapidly than that for HB wafers.

The market for LEC InP for optical devices is relatively small and is expected to grow from $10 million in 1985 to $50 million in 1990. Indium phosphide research has shown impressive progress in millimeter wave devices as well as in lightwave devices; however, the long-term growth of the market compared to GaAs cannot be reliably assessed. At present, there is only one small U.S. commercial supplier of InP.

TABLE 2.2 Worldwide Merchant Market Projections for III-V Semiconductor Materials ($ Million/Year)

Category	1985	1990	1995
Total III-V	120	420	920
GaAs	70	300	660
GaP	40	70	150
InP	10	50	110

Source: Private communication to the committee by T. Nakahara, Sumitomo Electric Industries, Ltd. (Japan), January 1987.

U.S. COMPETITIVE POSITION

There have been many studies of the U.S. competitive position in compound semiconductors and the electronic industry in general. All of these reflect U.S. concerns about the increasing Japanese presence in this industry [National Materials Advisory Board, 1986; Federation of Materials Societies, 1986; JTECH, 1985]. A common conclusion of each study is that in the past 5 years Japan has greatly increased its share of the compound semiconductor market and is beginning to dominate the technology in several key areas. The Japanese have targeted optoelectronics as a key technology, and their long-term objective is to claim a large market share.

One principal problem facing the United States in the GaAs arena is the need to establish manufacturing resources and the needed production experience that will significantly lower the cost of GaAs components. Although GaAs chips presently may have better performance than silicon, their cost can be as much as 10 to 20 times greater than that of a similar silicon chip. In some highly specialized, critical applications, cost is a minor limitation, and the material of choice depends on achieving exceptional performance. For most commercial applications, however, cost is a success-determining factor. Either the performance must be increased to justify the current price or the cost must be reduced to a level consistent with alternative technologies and with market demands for the available performance enhancements.

In a climate driven by profit, U.S. manufacturers are generally unwilling to invest large sums in manufacturing plants until a large generic market develops. Unfortunately, until a truly generic area that has very large volume potential is identified (either digital or linear), the costs per unit for GaAs parts will remain high. High-volume U.S. customers are rare today, so the economy of high production is absent, causing prices to remain high, which limits applicability, and so on.

In contrast, the Japanese have made a long-term, strategic commitment to compound semiconductor technology. As early as 1985, companies like Sumitomo Electric Industries and Dowa Mining Co. were already producing 10,000 2-inch GaAs wafers per month. Furukawa Mining Ltd., Iwaki Semiconductor, Mitsubishi Metal, and again Sumitomo Electric are all now shipping 3-inch wafers and targeted 4-inch material production for early 1987 (private communication to the committee by T. Nakahara, January 1987). In the area of devices, the Japanese are widening the gap with the United States in device manufacturability of complex parts. Examples are the NTT distributed feedback laser, the Oki Electric 8x8-bit multiplier, the NTT 16K static RAM, or the Fujitsu high-electron-mobility 16K memory operating at room temperature (four times faster than the equivalent 16K silicon part).

One key to Japanese pre-eminence in this field is dedication to manufacturability issues, where they are focusing on the design of cleanrooms, the right level of (robotic) automation, the use of on-line control and process feedback, and, perhaps most importantly, the proper level of investment in equipment development. The ability to make the proper long-range investment in equipment, processes, and people--whether it is in crystal growth, epitaxial growth, or strategically pure starting materials--is a true Japanese strength.

The committee estimates that the United States is well behind Japan in the optoelectonic sector and the digital logic sector of GaAs technology. In the field of linear, monolithic microwave ICs, there is approximate parity [Defense Science Board, 1987]. In the development of many of the processing technologies discussed in this report, the United States is trailing, and the gap is widening. It can be anticipated that, without any U.S. corrective action, Japanese superiority in compound semiconductor devices will mean eventual Japanese superiority in electronic and optoelectronic systems. Action is necessary to coordinate U.S. government, industrial, and academic resources in such a way as to reverse this erosion quickly and definitively.

PROPOSED SOLUTIONS

The committee feels that a strong U.S. position in compound semiconductor manufacturing technology is essential for future economic health in high technology. In the long term, compound semiconductors will clearly perform a critical complementary role to silicon technology. It is particularly dangerous to ignore the smaller near-term markets and permit overseas dominance. This will inevitably lead to U.S. inability to compete in large future systems markets. However, U.S. industry finds it difficult to make the necessary long-term investments. As a result, solutions will require government leadership.

In the committee's opinion, the following action warrant service consideration to strengthen U.S. competitiveness in the field of compound semiconductors:

- Establishment of a national review panel on compound semiconductors, consisting of members from industry, universities, and government. The functions of the panel should include (a) the formulation of a national strategy for compound semiconductors, (b) the coordination of research and development activities and funding, and (c) presenting recommendations for research and development actions. This panel should increase government agency, industrial, and academic cooperation in targeting and accomplishing significant goals, while eliminating duplicative programs.

- Establishment of a federal-commercial compound semiconductor technology center, funded at a sufficiently high level to attract

industrial participation. Its purpose would be to establish a common technology for the manufacture of compound semiconductor materials and devices for commercial and military use.

- Establishment of university research centers to train bachelor's, master's, and doctoral students in manufacturing technology. Such programs could include personnel and information exchange agreements with other technology centers.

These recommendations are essentially similar to those forwarded to solve the problems of the silicon industry, which indeed suffers from similar problems [McLoughlin and Miller, 1987]. However, the absence of a large existing market for compound semiconductor devices and the vital importance of these materials to future technology makes the case for federal support of compound semiconductor technology even stronger than that for silicon. Thus, all of the advantages considered in the proposed federal support of the SEMATECH proposal [Congressional Budget Office, 1987], such as overcoming the semiconductor industry's shortcomings in manufacturing technology and creating public benefits both in national security and commercial competitiveness, are especially applicable to compound semiconductors. At the same time the risks related to special advantages derived by member companies would appear to be reduced because of the immature state of the technology under development.

Federally administered centers concentrating on improving the U.S. innovative and manufacturing position in compound semiconductors also have been proposed in an IEEE and DARPA Strategic Materials Initiative and discussed in the recent Defense Science Board report on semiconductor dependency [Defense Science Board, 1987]. Legislation has already been introduced into Congress concerned with semiconductor manufacturing. Such legislation is viewed as an important first step toward strengthening the U.S. semiconductor industry. For compound semiconductors, this is particularly necessary, since the defense industry is currently the largest consumer of compound semiconductor electronic devices.

In the implementation of these recommendations, a most important component must be the coordination of research and development and the close coupling and feedback of the materials research with the processing and device fabrication communities. University research centers must be closely coordinated with the government and industrial centers. It is essential that these industry-university-government partnerships be selective, consistent, and planned with appropriate lifetimes to see the projects through from the start-up to a timely phase-out. It is also vital that the focus of the research be directed toward a commercial technology base, since this also is considered essential for a viable defense industry. The administration and staffing of new technology centers is an important issue requiring further study. The MITI-style approach [Merz, 1986] to sharing staff between such centers and industry has not been tested in the United States, where wide geographical differences exist.

PROCESSING CHALLENGES IN THE 1990s

In the following chapters of this report, the technical issues involved in the fabrication, reliability, and manufacturability of compound semiconductors are discussed. The chapters that follow begin with a discussion of device issues and then describes typical devices of current interest to provide an insight into the importance of each of the processing technologies, as well as an understanding of the unique advantages of compound semiconductors. The state of the art of each process technology is assessed, with emphasis on materials of greatest importance to the commercial development of future electronic and optoelectronic systems--namely, GaAs, GaAlAs, InP, InGaAsP, and HgCdTe.

Each of the processes of importance for device fabrication is discussed individually in succeeding chapters. Because of their great significance, separate discussions are devoted to issues of process control and the process environment, to interactions between the various processing steps, and to eventual device yield and performance.

In each case, current problems that need to be solved over the next few years are considered, and areas where fundamental understanding is deficient are identified. Attempts are made to identify the relationships between the material properties (defects, etc.) and processing procedures and the device performance and yield. Progress in this area of processing science will have immediate impact on manufacturing technology.

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CHAPTER 3

DEVICE ISSUES

PRINCIPAL RECOMMENDATIONS

Typical optical and electronic device structures of importance in compound semiconductor technology are described in this chapter, with particular emphasis on the processing issues that are critical to optimum device performance. It is vital that the device community fully recognize the importance of materials processing and testing for successful fabrication and operation of future high-performance electronic and optoelectronic devices.

Although most current commercial compound semiconductor devices are either discrete components or are used in relatively low levels of integration, the ultimate goal of compound semiconductor technology is the full integration of both photonics and electronics technologies for high-speed information processing and transmission. To achieve this goal, full control over the processing of discrete optical and electronic devices is an essential prerequisite. This chapter provides insight into why precise control of materials and process parameters is vital to the advancement of compound semiconductor technology.

The combination of different compound semiconductors in heterojunctions and small dimensions, where quantum effects dominate, has already led to a number of conceptual breakthroughs for new devices and circuits. Such breakthroughs are expected to continue. However, the ability to capitalize on new opportunities and make them a practical reality is severely restricted by current limitations in materials processing technology.

Subsequent chapters of this report deal with specific elements of materials processing. Recommendations for work appropriate to individual processes are made in relevant chapters. The following recommendations for future device processing are generic to optical and electronic technologies:

- Current electronics technology in compound semiconductors is based almost entirely on planar GaAs devices. Commercial realization of the advances offered by heterojunction technology for the next generation of ultrahigh-speed electronics requires a major commitment to materials processing and device fabrication of these structures.

- Integration of optical and electronic components on the same chip is essential if the full advantages of compound semiconductors are to be realized. This requires a focused effort to develop the required processing technologies.

- The use of novel interconnection techniques must be developed for low-loss and low-dispersion interconnection of high-speed integrated circuits. Optical interconnects and high-temperature superconductors should be urgently evaluated for this purpose.

- Detailed modeling must be developed for compound semiconductor devices and circuits to guide future development.

INTRODUCTION

This chapter strives to describe key materials and process parameters for the fabrication of electronic and optical devices using compound semiconductors. The device structures decribed demonstrate some of the basic building blocks of electronics and photonics technology and the complexity of the various processing steps required for manufacturable devices.

The evolution of compound semiconductor technology is summarized in Figure 3.1. The ultimate goals of this technology are the integration of both photonics and electronics technologies for high-speed information processing and transmission. At the present time, most commercial devices are either discrete components or are at relatively low levels of integration. Ultimately, as processing technology advances, increased levels of integration will provide a wide range of advanced circuit options for systems designers. For optoelectronic applications, compound semiconductors are unique, and silicon is not a competitive technology. However, for high-speed electronics, compound semiconductors must exhibit near-ideal characteristics to retain their anticipated performance advantage over silicon.

A comparison of the properties of several compound semiconductors with germanium and silicon is shown in Table 3.1. The mobilities quoted in the table are for undoped materials [Sze, 1981]. In practice, the mobilities may be considerably reduced from these values because of the high levels of doping required in some devices and because of electron scattering at defects and interfaces within device structures. It also must be remembered that in current high-speed VLSI circuit designs, interconnection delay between devices is sizable compared with device delay and represents a major limitation to circuit speed. Future emphasis must be placed on novel approaches to device and circuit interconnection if the real speed enhancements offered by compound semiconductors are to be achieved in VLSI circuits.

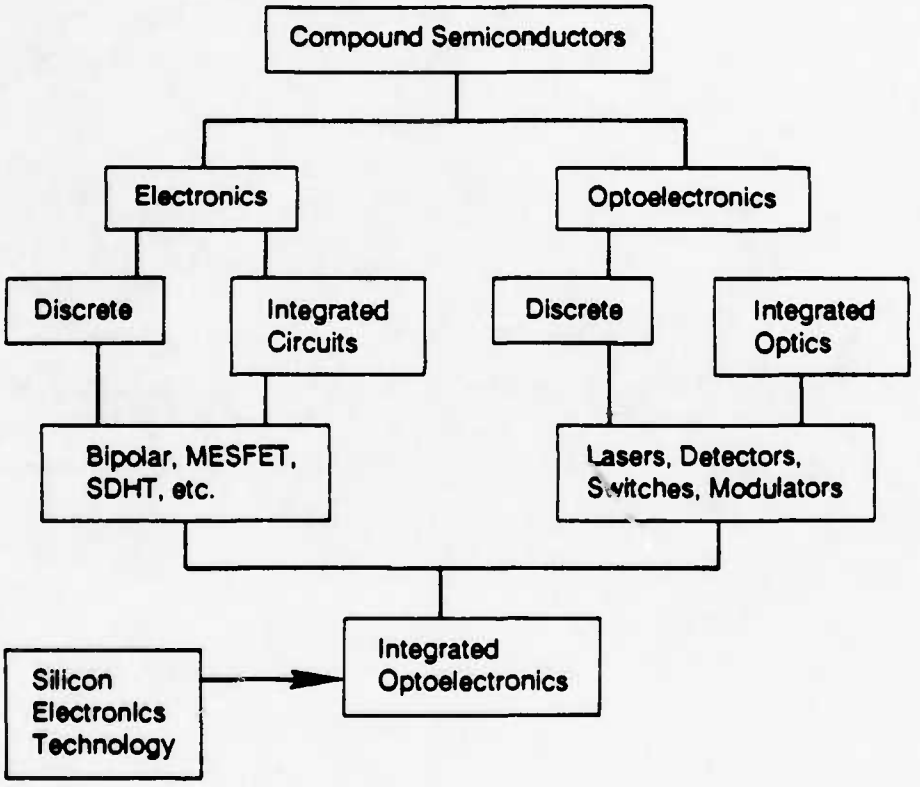


FIGURE 3.1 Evolution of compound semiconductor technology.

TABLE 3.1 Intrinsic Properties of Semiconductors

Material	Effective Mass[1] (m^*/m_o)	300 K Electron Mobility ($cm^2/Vsec$)	Energy Gap (eV)
Ge	1.64	3900	0.66
Si	0.98	1500	1.12
GaAs	0.067	8500	1.42
InP	0.077	4600	1.35
$In_{1-x}Ga_xAs$ (x = 0.47)	0.041	10000	0.81
$Hg_{1-x}Cd_xTe$ (x = 0.2)	approx. 0.01	35000	0.10

[1] m^* = effective electron mass
m_o = free electron mass

DISCRETE DEVICES

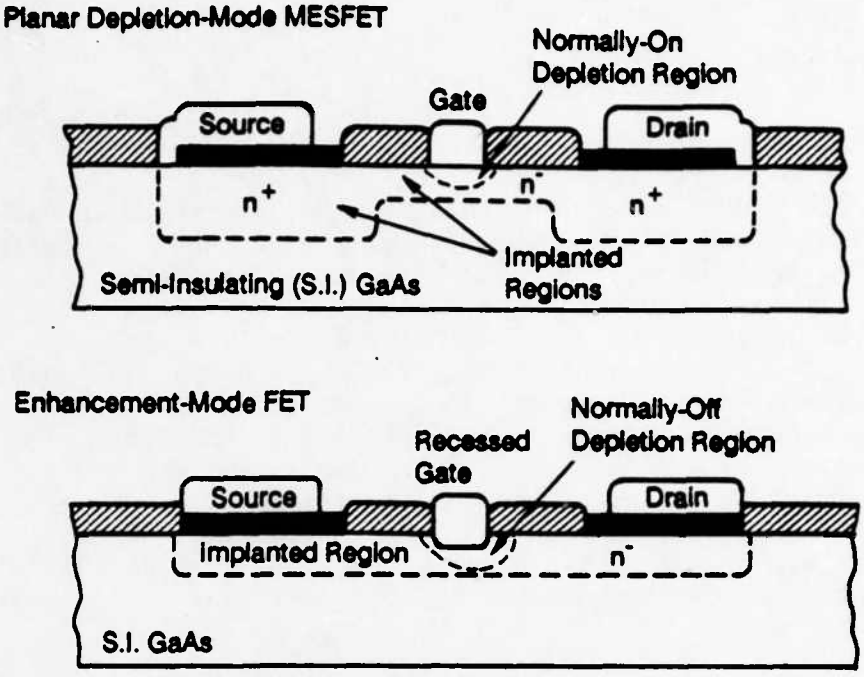
Transistor Structures

Metal-semiconductor field effect transistors (MESFETs) have been the most widely developed amplifying and switching devices using GaAs. These are dominantly made in a configuration on the surface of a wafer, as shown in Figure 3.2, with electrons moving under the surface from source to drain electrodes and a Schottky-barrier metal gate between these electrodes to control the current flow. Current flow between the source and drain is switched off when the channel is depleted of carriers at a specific gate threshold voltage. These "horizontal" devices are easy to integrate into microwave logic or optoelectronic integrated circuits. The thin GaAs conducting channel is formed on the surface of a semi-insulating substrate by ion implantation or epitaxy, which provides very low interelectrode capacitance for increased circuit speed. To increase device speeds, very short gate lengths that minimize electron transit times are required. With gate lengths of 0.25 to 0.50 micrometer, such devices can switch circuits in 10 picoseconds or can amplify signals to about 50 GHz.

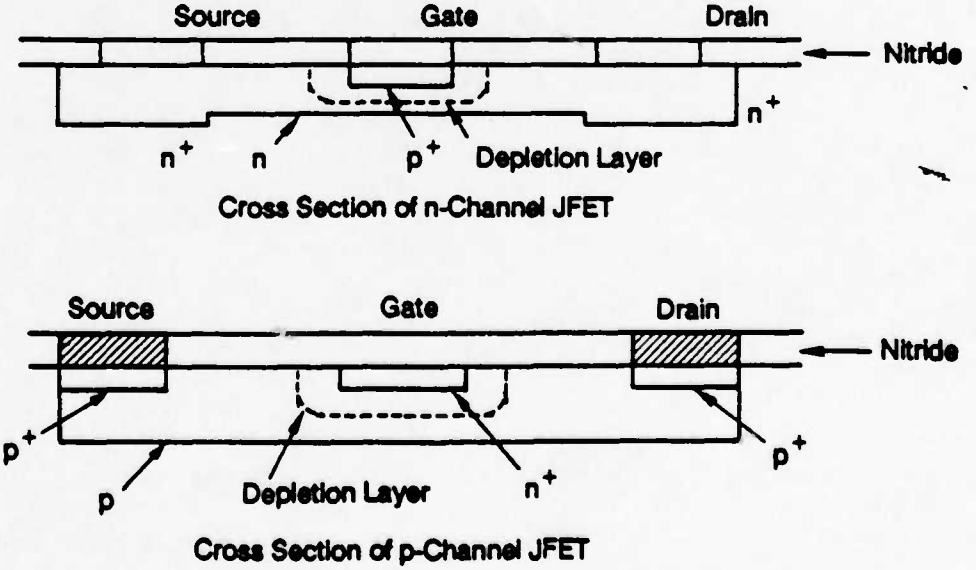
Devices with even shorter 0.1-micrometer gates are currently being studied. These gate lengths are smaller than can be reliably fabricated using present commercial optical lithographic techniques. Short devices (less than 0.5-micrometer gate length) require a potential barrier under the conducting channel to prevent performance degradation from space charge injection current coming from the source under the gate. When scaled to shorter gates, these devices require higher donor concentration, which increases the undesired collisions between electrons and ions. Collisions limit the electron velocity to a value just over 1×10^7 cm/s, so that the frequency response scales no better than the reciprocal of the channel length.

An additional limitation of this simple MESFET structure is that surface states at the metal-semiconductor interface limit device performance by trapping charge carriers. Furthermore, gate leakage currents arise due to the relatively low height of the Schottky-barrier. The height of the barrier could be greatly increased, and thus the gate leakage current greatly reduced, if an insulator is placed between the metal and semiconductor (MISFET). However, the absence of a suitable insulator on GaAs has prevented development of a MISFET technology.

Key advantages of InP over GaAs are possible with future development. Higher electron velocity (30 percent), higher thermal conductivity (40 percent), and higher breakdown voltage (50 percent) are among these advantages. Even more important is the fact that interface charges between InP and dielectrics on its surface are of much lower density than in GaAs. It is thus possible to accumulate a sheet of fast-moving electrons against this dielectric. This, along with higher breakdown



(a) Metal semiconductor FETs or MESFETs (courtesy of Rockwell International)



(b) Junction FETs or JFETs (courtesy of McDonnell Douglas)

FIGURE 3.2 Examples of horizontal field effect transistor (FET) structures

voltage, in turn allows high-peak microwave power generation with InP MISFETs. InP technology is also an excellent base for heterojunction FET and bipolar transistors of the type described later.

MESFET structures can be made with vertical geometries, where electrons go from a buried source layer through a thin channel layer to a top drain electrode. In such a structure, the effective gate length and electron transit time through the base region are greatly reduced and can be precisely determined during the epitaxial growth process rather than by lithography as in the horizontal FET. However, the parasitic capacitance and resistance of this structure become the major speed limitation. Metal gates placed between the source and drain can control the current flow. A version of this device known as the permeable base transistor (PBT) has been successfully demonstrated at the M.I.T. Lincoln Laboratory after the difficult technology of constructing it was mastered. Its frequency performance was over 20 percent higher than any horizontal MESFET. This was caused by its short vertical channel, which is grown epitaxially rather than being formed lithographically as in the horizontal MESFET. Unity power gain frequences for these devices are 180 GHz and 220 GHz, respectively, for the MESFET and PBT.

Using heterojunctions, both the horizontal FET (Figure 3.3) and the bipolar (Figure 3.4) transistor are significantly improved. Using doped $Al_{0.3}Ga_{0.7}As$ on undoped GaAs as an example, the donor ions in the larger-band-gap alloy neutralize the space charge of the electrons in the GaAs. The electrons in these modulation-doped FETs (referred to as MODFET, SDHT, and HEMT devices) form a two-dimensional electron gas at the heterojunction interface and have a 0.24-eV confining barrier between them and the ions in the barrier region. The electrons have few collisions when moving parallel to this heterojunction and hence move faster than they would in an equivalently doped channel.

MODFETs have demonstrated switching times in circuits as short as 5.8 picoseconds at 77 K and excellent performance in high-speed logic. Microwave circuits have achieved a noise figure and current gain cutoff frequency superior to that of GaAs MESFETS [Drummond, et al., 1986]. By using a limited amount (about 15 percent) of indium in the GaAs in a thin layer, the potential barrier can be raised to about 0.30 eV for even more advantage, in spite of the small-lattice-mismatch strain [Rosenberg et al., 1985]. Indium alloys can eliminate problems arising from donor-related electron traps (so-called DX centers) in doped AlGaAs with high aluminum content. With a 0.25-micrometer gate length, these devices have been tested to yield a unity power gain frequency of 230 GHz. The barrier height can be increased to 0.5 eV by growing $In_{0.52}Al_{0.48}As$ wide-bandgap material on $In_{0.53}Ga_{0.47}As$ that in turn is grown on an InP semi-insulating substrate [Kuo et al., 1987]. A very-high-performance MODFET is possible with this structure. When fully developed, this device will also have superior unity-power-gain frequency.

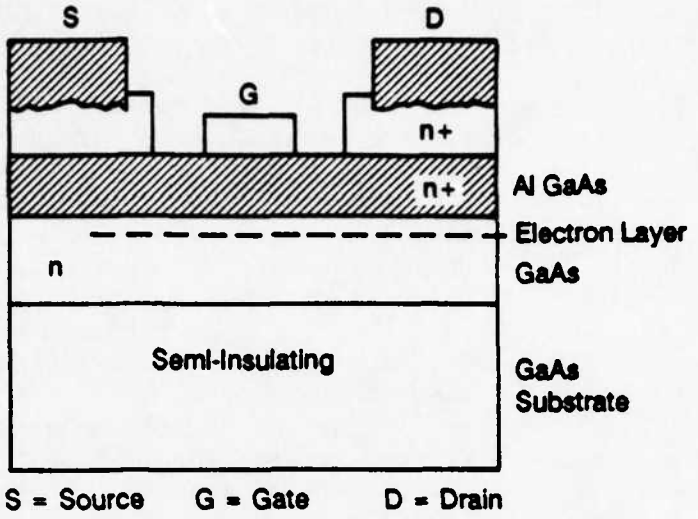


FIGURE 3.3 Schematic of Horizontal FET.

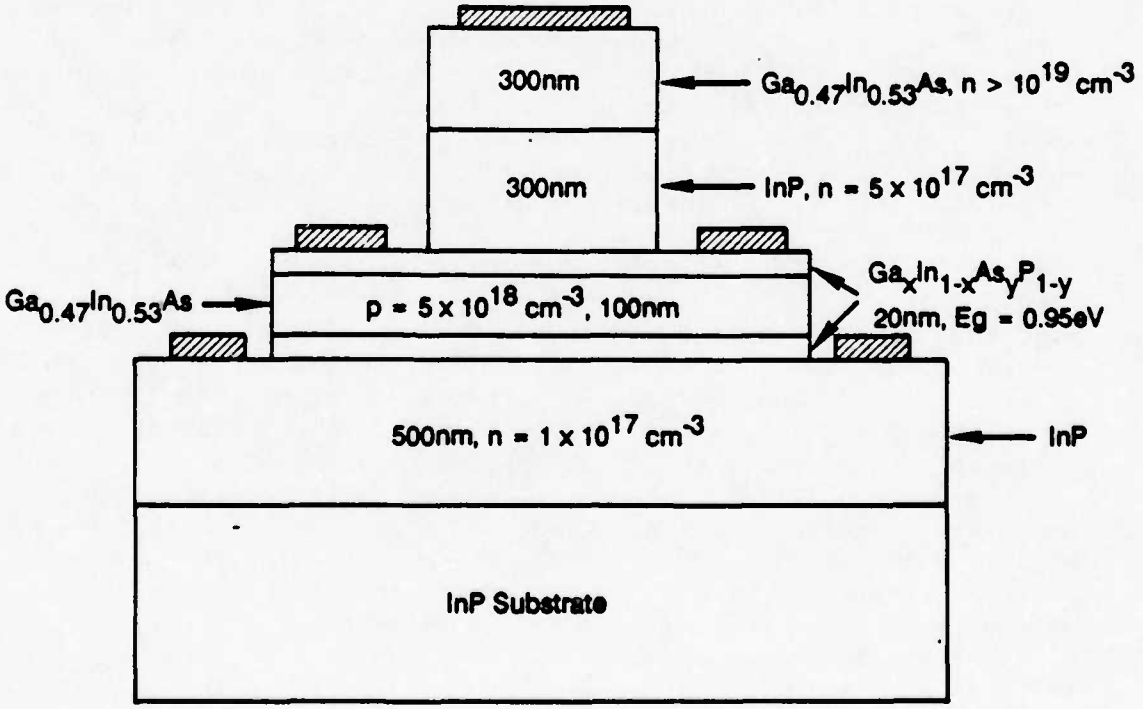


FIGURE 3.4 Schematic of a Bipolar FET.

When an $Al_{0.3}Ga_{0.7}As$ n-type emitter is used in an otherwise GaAs n-p-n bipolar transistor, there are strong advantages. High current gain can be achieved, even when heavy acceptor density levels are used in the base. This effect results from the heterojunction at the emitter-base interface limiting the hole injection into the emitter. Unity-power-gain frequencies as high as 105 GHz have been reached with a 1.2-micrometer emitter. These devices presently operate at a current density of 4×10^4 A/cm^2. Such high current densities allow small area devices to switch very dense and loaded logic circuits at high speed.

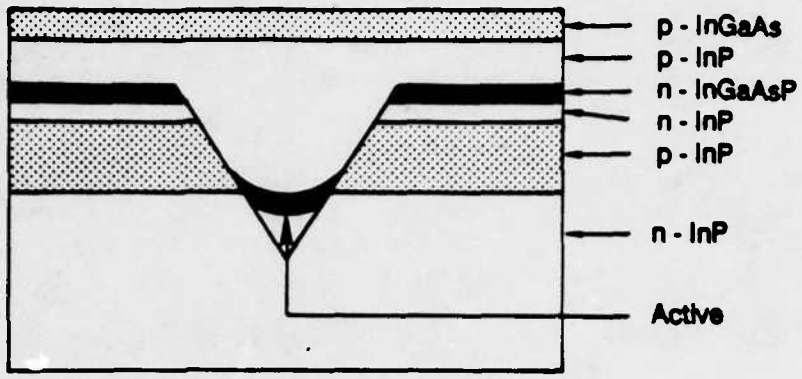
The speed of such bipolar transistors is still limited by extrinsic factors such as junction capacitance and not by the carrier transit time. For this reason it is most important to reduce the lateral dimensions of the transistor to obtain higher speeds and lower power requirements. However, decreasing the dimensions results in increased surface recombination, which limits current gain. This is particularly serious in GaAs. Techniques to reduce the surface recombination velocity are essential to future progress in this direction.

An interesting set of vertical transistors using hot electrons, and even ballistic electrons, is being investigated. Tunneling and resonant tunneling of electrons are used in some of these devices. Breakthroughs could lead to transistors with unity power gain frequencies up to 1000 GHz and switching times down to 2 picoseconds. There would be substantial technological difficulties in the integration of these vertical devices, which would require further effort in materials growth and device fabrication.

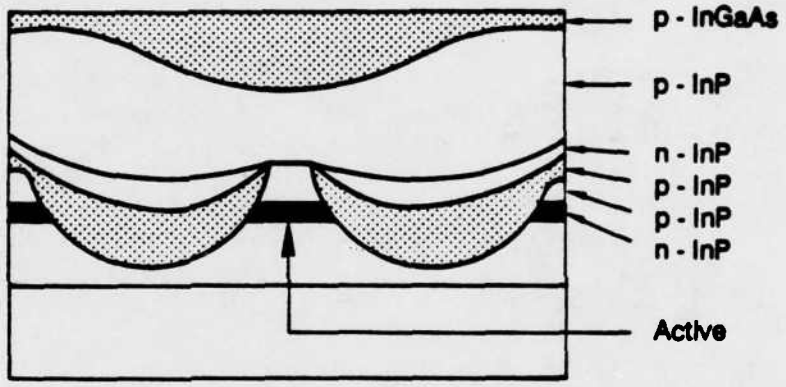
Lasers

Both GaAs-GaAlAs and InP-GaInAsP material systems play major roles in current laser technology. GaAs-based devices operate at wavelengths shorter than 0.88 micrometer and are suitable for consumer products and short-distance communication. For longer-distance communication, InGaAsP-based devices operating at wavelengths of 1.3 and 1.55 micrometers are essential to match the wavelength of minimum dispersion and minimum loss of silica optical fibers. Fiber loss at 1.55 micrometers is only about 10 percent of that at 0.88 micrometer. The use of these longer-wavelength devices for short-haul applications depends on the eventual relative cost of the two materials and various systems requirements.

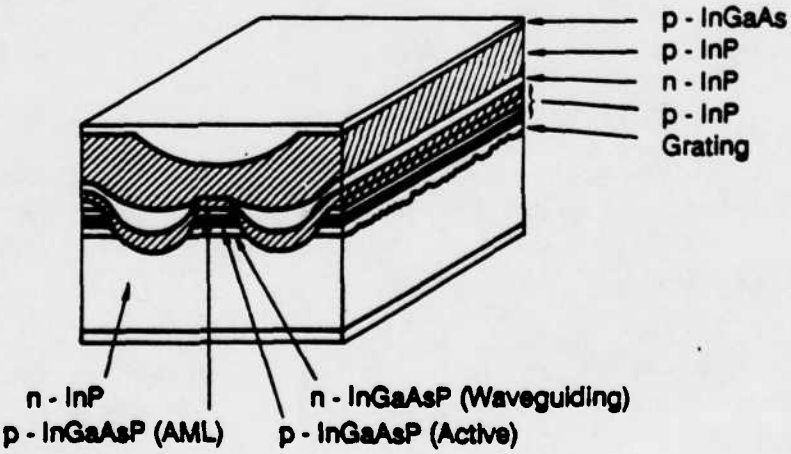
Lasers are probably the devices most sensitive to the quality of the substrate and epitaxial layers. Laser reliability is sensitive to imperfections in the laser structure. The simultaneous presence of very high current densities and optical intensities result in laser degradation unless the material quality is exceptionally high. Typical laser structures of commercial importance are shown in Figure 3.5. One of



(a) The crescent-substrate-buried heterostructure (CSBH)



(b) The double-channel planar-buried heterostructure (DCPBH)



(c) The distributed feedback DCPBH

FIGURE 3.5 Examples of laser structures.

these is a channel-substrate-buried heterostructure (CSBH) in which the active region of the laser is grown inside a groove etched into the substrate prior to layer growth. Another is a dual-channel-planar-buried heterostructure (DCPBH) in which the active layer is grown on a planar substrate, followed by etching of two channels through the layer into the substrate on either side of a mesa. The structure is then completed with a second growth step that fills the channel and caps the entire structure. These structures are designed so that the current flows through the active lasing region only. Either reverse-biased p-n junctions (as shown in Figure 3.5) or semi-insulating layers (not shown) block the current in surrounding regions. In both of the structures shown, the curvature of the layers is the characteristic solidification from solution in LPE growth. Mesa structures, similar to the DCPBH, can be adapted for vapor phase growth.

Key processing considerations common to most laser structures are as follows:

- The width and uniformity of the etched channels to submicrometer tolerances is critical for minimum optical loss and proper transverse optical mode control. The features must be preserved during the layer growth.

- Epitaxial layers must be grown with precise composition control to give good lattice match to the substrate (less than 0.1 percent), low misfit dislocation density, and low stress levels. Laser lifetime and reliability is considerably reduced if stress from any source (substrate mismatch, metallization, dielectric, bonding, etc.) exceeds about 1 x 10^9 dynes/cm^2, or if even a single defect occurs in the active region. Composition control and uniformity are also essential for tight control of the emission wavelength and spectral width of the laser line.

- The epitaxial layer thicknesses must be controlled to better than 0.1 micrometer for good optical mode control.

- The dopant levels are critical for proper placement of the p-n junctions within the active layer.

- High material purity and structural quality are essential for long minority carrier lifetime and low density of nonradiative recombination centers.

- With lasers, it is particularly vital that the deposition of dielectrics for masks and facet coatings (to prevent facet degradation) be done with low damage and at low temperature to preserve the surface composition and structure of the semiconductor.

- Since lasers typically operate at several kA/cm^2, metallization must be ohmic and must not migrate into the semiconductor during bonding or during device operation.

The degree of process control required increases as the requirements for laser stability, line width, and mode control become more stringent. The very narrow laser line width necessary for high-bandwidth, low-loss communication systems requires longitudinal mode control in the laser structure. The distributed feedback (DFB) laser achieves this with a periodic grating etched into the substrate prior to the growth of the laser. In such a structure, both the grating amplitude and the thickness of the epitaxial layers above the grating affect the resonant frequency, so extremely precise control of the etching and crystal growth are essential. Aging effects, in which the gain peak of the laser shifts with time, give rise to catastrophic degradation of the performance of this device. This is also true in laser structures that have the frequency-selective element external to the laser cavity.

Future communication systems will likely incorporate coherent detection, which offers about a hundredfold improvement in detection sensitivity over direct (incoherent) detection. This is accomplished by heterodyning the received weak carrier signal with a strong local oscillator. Distributed feedback lasers do not have sufficiently narrow line width for this application. Laser line narrowing must be achieved with feedback from external optical elements. External modulation and wavelength tunability will probably be required for such systems. This might actually relax the requirements on the laser itself because direct modulation of the laser would no longer be required.

Detectors

Detectors are subject to much less stress than lasers (i.e., low current density, low intensity) and, as such, are less subject to long-term degradation. Nevertheless, to achieve the optimum performance from detectors, particularly avalanche photodiodes, careful control of the processing is required.

Two kinds of detectors are generally considered for optoelectronic applications. These are junction (PIN) photodiodes and avalanche photodiodes. For far-infrared imaging applications that use narrow-gap materials, photoconductive and photovoltaic detectors are commonly used. Silicon detectors are generally used in conjunction with GaAs-GaAlAs lasers. Either InGaAs or germanium detectors are used with longer-wavelength InGaAsP lasers.

Typical long-wavelength PIN and avalanche photodiode structures are shown in Figure 3.6. In each case, the absorbing layer is 2 to 4 micrometers thick and is grown on an n-type InP substrate. A thin layer of wider gap material is grown over the InGaAs to reduce surface leakage currents, and this in turn is coated with a dielectric passivation layer. To form the p-n junction, acceptors such as cadmium or zinc are diffused into the InGaAs absorbing layer through a small opening in the cap layer.

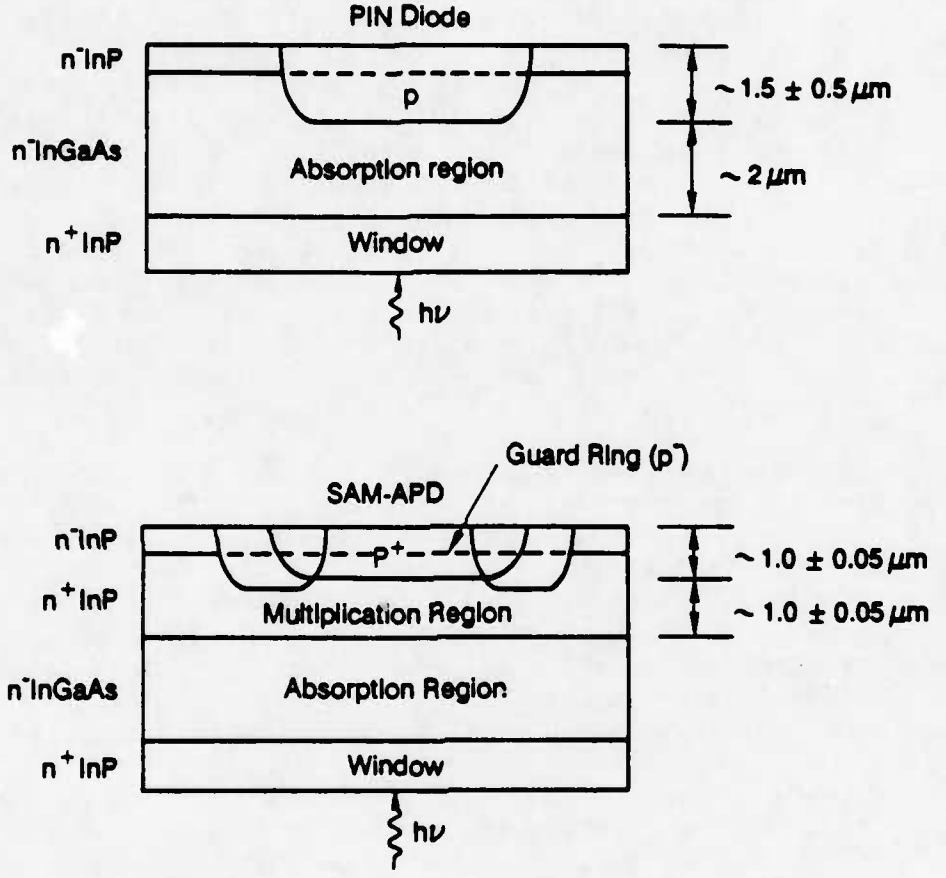


FIGURE 3.6 Schematic of two detector structures: The PIN Diode and the SAM-avalanche photodiode.

Under reverse bias, the absorbing region is depleted of carriers. Since the junction region is generally illuminated through the InP substrate for maximum efficiency and bandwidth, it is necessary to have low substrate absorption.

There are two key factors in fabrication of PIN photodiodes: (a) the absorbing InGaAs layer must be extremely pure to achieve full depletion of the layer at low voltages and to minimize junction capacitance, and low voltages are required to minimize noise due to tunneling; and (b) the surface passivation dielectric must be deposited with minimum damage and strain, and the epitaxial layer quality must be sufficiently high for mimimum dark current.

Good photodiodes are shot-noise limited, with near-unity quantum efficiency and bandwidths exceeding 10 GHz, limited by the RC time constant of the detectors and receiver circuit. For wide-bandwidth systems, however, amplifier noise is dominant, and in practice this noise level is some two to three orders of magnitude greater than quantum noise (approximately 20 photons per bit for an error rate of 10^{-9}). To obtain the highest possible signal-to-noise ratio, the signal from the photodiodes should be as large as possible. Sensitivity can be improved with avalanche photodiodes with internal gain to increase the signal level before the addition of preamplifier noise.

Narrow-gap semiconductors have a large background leakage current, at the high reverse voltages necessary for gain, due to tunneling from valence to conduction bands. To get around this problem, heterostructure APDs are fabricated, as in Figure 3.6, in which the absorption layer is a thin InGaAs layer and the avalanche gain occurs in the wider-gap InP. The electric field in the absorbing layer is sufficiently low to prevent tunneling currents in that region but high enough to achieve avalanche multiplication in the InP region. These devices are referred to as SAM-APDs (separate absorption and multiplication regions).

The difference in the valence band of 0.4 eV at the heterointerface leads to hole trapping and reduced performance. A graded-bandgap region of InGaAsP can be grown between the absorption and multiplication region to eliminate this problem. Such structures place very strenuous demands on degree of control required for epitaxial growth.

To obtain high performance, APDs involve further processing issues in addition to those for PINs. To obtain a high-gain-bandwidth product, the p-n junction depth and uniformity are critical to within 50 nm. To obtain uniform gain across the detector area, the planar device shown in Figure 3.6 requires a guard ring to prevent breakdown at the edge. These structures require extremely high precision. Even slight deviations in layer thickness, uniformity, or carrier concentration can result in drastically high leakage currents. Dislocations threading through the epitaxial layers can give rise to microplasmas in the high field regions. For this reason, only a few such commercial devices are available.

Germanium APDs, which are sensitive in this wavelength range, are commercially available in Japan and have proved to be very reliable. The dark currents are, however, higher than the best InGaAs SAM-APDs. For sufficiently high gain, the noise of APDs becomes the dominant receiver noise. This noise is due to the avalanche process itself and not quantum noise. The lowest excess noise is achieved when the ionization ratio of holes to electrons becomes small. In InP, this ratio is about 1 to 3 and in germanium about 1 to 2. In certain HgCdTe compositions and some InGaAsP superlattice structures, however, the ratio can become extremely small in the 1.3- to 1.6-micrometer spectral range, which in principle could result in APDs with very low excess noise. Reliable devices with these characteristics have yet to be fabricated.

Coherent detection schemes exhibiting close to quantum noise-limited detectivity have been demonstrated in the laboratory and offer the greatest promise for ultimate sensitivity. For such applications, shot-noise limited PIN detectors will likely be the devices of choice.

SIZE SCALING ISSUES

Lateral control of dimensions is best illustrated by the MESFET and MODFET examples. Dimensions of the gate electrodes will be gradually reduced from 1.0 micrometer down to at least 0.5 micrometer for digital circuits and to 0.1 micrometer for microwave circuits. The MESFET channel thickness will be reduced by approximately the same amount, thereby becoming smaller than the gate length. The doping in the channel will rise in proportion to the reciprocal of the gate length. MODFETs have thin (100 nm) electron sheets that are brought closer to the metal gate to achieve shorter gates. Quantum limits are imposed on the thinnest electron sheet dimension, even for the doping channel. Confinement of these electrons by a heterojunction or other potential barrier beneath the electron sheet also will be required to prevent unwanted space-charge injected current under this sheet. The gaps separating the gate from the source and drain will also be reduced proportionately. Alignment of these different parallel electrodes will become very difficult. There should be self-alignment schemes developed for these devices so that a high yield can be obtained over a large wafer that is densely populated with devices. Lateral diffusion of impurities, such as those that are ion implanted for self-aligned ohmic contacts, must be controlled. The ohmic contacts must also be controlled so that lateral motion of the metal does not affect either the yield or the reliability.

The control of the vertical structures, such as doping and composition profiles, must also be established for electron confinement to quantum wells and for reliable performance. Device breakdown conditions, especially in the presence of diffusing or drifting impurities, must be maintained. Diffusion studies to establish the best dopants and compositions for reliability are required.

DEVICE AND CIRCUIT MODELING

Much work is necessary to develop useful models in two and even three dimensions for small devices. Submicrometer dimensions yield different and improved electron transport properties where the electrons can approach ballistic motion. For dimensions under 500 nm, there are even quantum mechanical considerations. Increased current densities and space-charge injected currents need to be studied for the resulting high-speed and high-frequency devices.

INTEGRATION OF DEVICES

Integrated Electronics

High-speed digital electronics require small-area devices that are closely spaced. This places severe requirements on the devices, on their construction, and on heat removal. FET devices should achieve the highest possible current densities, with a goal of greater than 1 A/mm, so that small periphery devices can drive interconnection lines. Heterojunction bipolar devices should also have high current values, with a goal of greater than $10^5 A/cm^2$, for the same reason. Good noise margin requires reasonably high input voltage capability that is not readily available yet from MESFETs but is available in some forms of MODFETs.

Microwave and millimeter-wave integrated circuits will require high cutoff frequency and either low noise or high power. For low noise, extremely low contact resistance, channel resistance, and gate resistance are required. For high power, a high drain-to-gate breakdown voltage (15 to 25 V) is required, in addition to high current density (0.5 to 1.0 A/mm). The MESFET has performed well to 40 GHz, while the MODFET has performed well to 60 GHz. In the latter case, a noise figure of 2.3 dB and power density of 0.4 W/mm at 28 percent power-aided efficiency have been obtained at 60 GHz. Various circuit elements are required in addition to the transistors, and these can be constructed from metal patterns on the microwave and millimeter-wave integrated circuits. These elements are portions of transmission lines and even part of quarter-wave dipole antennas for signal radiation.

Optoelectronic Integration

Most commercial optical devices today are discrete devices fabricated by liquid phase epitaxy. Simple devices such as the CSBH laser and PIN detector can be made with high yields, so that thousands of discrete devices can be fabricated on a single substrate. More complex laser and APD structures cannot be manufactured with such high yields, but rapid progress is being made in this area.

Considerable effort is being directed toward the integration of optical and electronic components on the same chip. The drive toward device integration is to attain increased functionality and lower device cost. (At present, much of the device cost is in testing and packaging, which is reduced by integration.) However, device integration becomes economically worthwhile only when processing technology is sufficiently advanced to provide high device yield.

Integration of devices places some limitations on the device design. A semi-insulating substrate or blocking layer is required to isolate devices on the same wafer. Contact must be made to various levels of the device structure by selective etching from the upper surface. Planar laser and detector structures must be fabricated on the semi-insulating surface, and facets must be exposed by etching techniques. These processes are still at an early research stage and need extensive development.

A variety of integrated optoelectronic devices such as PIN-FET receivers, FET-laser transmitter chips, and optical repeaters already have been fabricated in the research laboratory. Coupled laser arrays that deliver high output power have been fabricated. Linear laser and detector arrays for coupling to several fibers in parallel have been demonstrated. The range of possibilities is great, and new prototype devices for optical processing and interconnection are being demonstrated constantly. As the degree of integration of devices increases, so does the importance of process control. Full control of the processing of discrete optical and electronic devices is an essential prerequisite for the high-yield fabrication of integrated device structures.

Materials Integration

Full integration of optics and electronics technologies ideally requires the integration of the various materials systems on a single substrate. Monolithic integration of III-V and II-VI compound semiconductors on silicon substrates will permit the different advantages of each material system to be used in a fully compatible way. Considerable material research and development currently is aimed toward that goal--particularly the epitaxial growth of GaAs on silicon. Because of the different crystal structure and lattice parameters of the various compounds, pseudomorphic epitaxial growth is possible only with very thin films in which the structure is strained to match the lattice parameter of the substrate. In thicker films, the strain relaxes by the formation of dislocation at the interface. Future research is needed to fully assess the effects of the strain and defect structure and to minimize their effect on device performance.

INTERCONNECTIONS

As the density of components in integrated circuits increases, so does the complexity of interconnection between devices and between chips. For very-high-speed circuits, interconnection becomes a serious limitation because of delays and frequency-dependent attenuation in the transmission line. In normal conductors, the skin depth decreases as the inverse square root of the frequency, with a corresponding resistive loss increase and decrease in frequency response.

A second problem involves the large electrical power needed to charge the transmission lines. One solution to these problems is to use optical pulses in fibers or waveguides. Such transmission lines have negligible loss and dispersion for computing applications, and no charging of the transmission line is necessary. Converting electrical information to optical pulses involves placing LEDs or lasers at key positions in the integrated circuit. For this reason, a monolithic technology that incorporates electronic and optical devices on the same chip is highly desirable.

A second approach worth investigating is the use of superconducting transmission lines, in which loss and dispersion is (at least in principle) greatly reduced. The new high-temperature superconductors may be useful for this application, but, at present, little information is available on loss and dispersion in these new materials. The penalty paid in cooling the circuits to liquid nitrogen temperature may be acceptable in future high-speed circuits, since significant increase in the semiconductor mobility and device speed is also achievable on cooling.

PROCESSING REQUIREMENTS

The materials processing requirements for both optical and electronic devices and integrated circuits are generically similar. Precise doping profiles are required to achieve uniformity over large wafer areas and reproducibility. Heterojunctions requiring composition control and with very abrupt interfaces will be required for the next generation of electronic devices as well as optical devices. Material properties will be engineered through use of varying alloy compositions, heterojunctions, quantum wells, and superlattices formed by epitaxial growth. In addition to the more common lattice-matched heterojunction, thin pseudomorphic layers of lattice-mismatched materials will be very useful. In some cases, structures will be required that do not have their junctions or interfaces parallel to the substrate, as found in conventional epitaxially grown layers. Layers must be regrown after grooves or other depressions have been etched into the original surface. Such regrowth or other reprocessing of critical active regions of devices, while common in discrete laser structures, is only in its infancy in integrated circuits and requires substantial future effort. The surfaces of compound

semiconductors and their interfaces with dielectrics also need substantial effort to prevent formation of unwanted sheets of charge and to provide chemical stability for device reliability.

High-throughput epitaxial growth systems with reasonable capital costs will be essential to obtain cost-effective integrated circuits using heterojunction devices. In order to utilize heterojunctions for high-performance devices and integrated circuits, it will be necessary to develop an affordable, controllable advanced processing technology.

Key dimensions of transistor elements during the next few years will be in the submicrometer range, down to 0.1 micrometer. Lithography with electron or ion beams or x-rays will be necessary. Electron-beam lithography is slow and may not be cost-effective for dense integrated circuit fabrication. Hydrogen ion beam lithography can yield a hundredfold increase in writing speed over that of electron beams. Both of these swept beam lithographic methods will have in situ alignment near critical electrodes for active sensing and alignment. Once masks are made, x-ray lithography is a rapid means of fabrication of submicrometer structures as long as alignment and mask rigidity are assured. Combinations of x-ray lithography and beam lithography, for the proper location and control of size of critical electrodes, can be of great benefit in obtaining satisfactory throughput.

Dry processing needs to be more fully studied for application to compound semiconductor devices and integrated circuits. Selective etching, damage to the semiconductor surface, and the removal of unwanted by-products all need further effort.

Today, there are no fully satisfactory insulators for compound semiconductors. The need for passivation without uncontrolled interface charges is essential. There may even be substantial advantages for compound semiconductor MISFETs if a proper insulator is developed. Such an insulator would be chemically stable with the compound semiconductor and would not have an uncontrollable interface charge. With such MISFETs, very-high-current density, increased noise margin, and complementary circuits should be possible. The high current would make more competitive logic devices with reduced periphery, as well as high-power microwave devices. Metallization of compound semiconductors also must be advanced. Schottky-barrier gate metals that are refractory and could withstand elevated operating temperatures would improve performance and reliability. Ohmic contacts that are formed without melting (during alloying) will be essential for reliability and closer spacing without shorting devices during processing or in subsequent operation.

During processing, elevated temperatures used can cause diffusion of impurities or interdiffusion at heterojunctions. Ion bombardment that occurs during ion milling, sputtering, or plasma etching can cause damage that must be annealed away at elevated temperatures. The strain caused by

the differences in thermal expansion of the semiconductors and their metallization and dielectric coatings can also cause changes in device performance due to piezoelectric effects common in compound semiconductors. Chemical reaction on the surface or the movement of surface metallization also can be problematic during processing. Subsequent chapters address each of these processing issues in detail.

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CHAPTER 4

BULK SINGLE CRYSTALS AND SUBSTRATES

PRINCIPAL RECOMMENDATIONS

The consistently repeatable production and availability of GaAs and other III-V compound single crystals with the same chemical and electrical characteristics that will yield devices with reproducible electronic characteristics remains the most critical problem in III-V compound device technology. The following recommendations are aimed at improving substrate technology:

- Coordinate R&D on the detailed relationships among crystal growth parameters, defect structure, and electronic characteristics of single crystals. Close interaction between substrate users and suppliers must be established.

- Develop wafer-scale characterization techniques for rapid evaluation of the important wafer parameters in a production environment.

- Establish substrate specifications for reliable device fabrication.

- Conduct comprehensive studies of the thermodynamics and the formation and interaction kinetics of lattice defects in compounds, since these are the primary factors affecting the electronic behavior relevant to device performance.

- Develop techniques for automated processing, maintenance of clean low-damage surfaces, and wafer packaging.

BULK CRYSTAL GROWTH

The potential of semiconductor compounds for electronic applications (particularly that of GaAs) has been recognized and demonstrated during the past 30 years. Yet the quality of single crystals available today for the fabrication of device structures is still poor in terms of chemical composition and defect structure. This poor quality prohibits the reproducible fabrication of reliable and demanding structures that, as already stated, not only are commercially important but also, in many instances, are critical to national defense systems. Ultimate progress in the performance and complexity of device structures can be directly

related to progress in the chemical and structural perfection of single crystals.

Growth Methods and Availability of Bulk Single Crystals

Two principal methods are currently in commercial use for the production of single crystals, the Bridgman and Czochralski methods [Brice, 1965]. In the Bridgman method, crystals are solidified by slowly moving the charge through a thermal gradient. Growth is initiated at a seed crystal placed at the coolest end of the melt. In the liquid-encapsulated Czochralski (LEC) method, a rotating seed crystal is dipped into a melt from above and slowly withdrawn as a crystal solidifies on the seed; the liquid encapsulant, usually boric oxide, is used to minimize decomposition of the melt during growth.

For GaAs growth, the Bridgman technique, in a horizontal geometry (HB), is the least expensive and accounts for about 80 percent of world sales. The compound is generally synthesized from the elements in the same silica boat as that used for subsequent growth. Equilibrium conditions are achieved in the melt by controlling the arsenic pressure with a second temperature zone, avoiding the need for encapsulation. Crystalline boules grown this way have a D-shaped cross section.

Undoped semi-insulating GaAs for the fabrication of integrated circuits is grown by the Czochralski technique. In this technique, the thermal gradients at the growth interface are higher than with the HB technique. These gradients give rise to thermal convection and thermal strains, and these in turn result in dislocations in the crystals. Considerable effort has been devoted, primarily by the Japanese, to reducing convection and increasing crystal perfection by decreasing thermal gradients through the use of magnetic fields and computer control of the growth conditions.

The high pressure of phosphorus that exists over an indium phosphide melt renders the conventional Bridgman method unsuitable for the growth of InP (or GaP) crystals. These crystals are commercially grown by LEC. However, a recent report [Gault et al., 1986] has shown that growth of InP by vertical-gradient freeze produces undoped single crystals of higher quality than LEC by lowering the thermal gradient at the growth interface. This technique is also suitable for GaAs.

Origins of Chemical and Structural Defects

Regarding the quality of today's single crystals, the following comments, although generally applicable, are specific to GaAs crystals. Its defect structure and electronic characteristics are very inconsistent

both within a given crystal and from crystal to crystal. This lack of uniformity and reproducibility represents one of the major yield-limiting problems of the GaAs industry. The issues of concern include the following:

- The level of chemical purity of the crystals not only is unsatisfactory but also varies. Carbon, heavy metals, and other residual impurities are commonly present and lead to changes in carrier concentration, in compensation ratio, and thus in carrier mobility. These impurities originate either in the starting elemental materials or are introduced during crystal growth.

- Deviations from stoichiometry are readily encountered in all materials with a volatile constituent. Their effects on the electronic characteristics, as related to defect structure, are very pronounced, even for departures from stoichiometry of a small fraction of a percent. The level of activation of ion-implanted impurities in GaAs is very sensitive to the arsenic stoichiometry--indeed, the highest levels of activation are observed in arsenic-enriched crystals. The thermal stability of GaAs during device fabrication (such as variation of surface resistivity following wafer annealing) is critically dependent on stoichiometry.

- The defect structure in compound semiconductors is extremely complex. Point defects (vacancies) are invariably incorporated during the growth from the melt. Deviations from stoichiometry lead to the incorporation of excess point defects. Depending on the Fermi level and the rate of cooling, point defects interact to form complexes that are electronically active (shallow and/or deep levels). Regarding line defects (dislocations), thermal stresses become important, in addition to the Fermi level position and rate of cooling. The Fermi level determines the charge occupancy of the point defects and thus their tendency to interact and also to coalesce. These defects can then affect the performance of devices.

Line defects (dislocations) continue to be a major problem in semiconductor compounds. Dislocations are produced in crystals during growth either by thermally induced stresses or by point defect coalescence. Doping crystals can reduce dislocations by increasing the critical shear stress (hardening the lattice). Isoelectronic doping--e.g., In-doped GaAs [Jacob et al., 1983]--has been found to decrease substantially the dislocation density without affecting the resistivity of the wafers, but it is not yet clear whether this type of doping represents a desirable solution to the dislocation problem.

Impurity hardening has problems, including reduced wafer yield from a crystal run and changes in the lattice dimension compared to GaAs. The yield problem is a direct result of the fact that the dopant used to harden the lattice, such as indium, does not have a distribution constant near unity. As a result, each segment of the boule from the seed to the

tail has a different dopant concentration [Kimura et al., 1984]. Near the end of the GaAs/In crystal growth process, the boule becomes polycrystalline generally due to constitutional supercooling. The alternative preferred solution to decreasing the dislocation density is to grow crystals in a reduced thermal stress environment--low thermal gradients and reduced convection.

Device Structure Problems Related to Bulk Crystals

Epitaxial Structures

Electronic devices can be fabricated either directly as the substrate crystal or alternatively in epitaxial layers grown on top of the substrate. The current-generation integrated circuit structures most commonly are fabricated directly in semi-insulating GaAs, using ion implantation to define conducting channels. More complex integrated circuits, such as heterojunction, bipolar, or modulation-doped devices, and all optical devices, are fabricated in epitaxial layers.

For many years the view was held, and still is in some quarters, that epitaxial structures are not affected by the quality of the substrates on which they are fabricated, particularly if buffer layers are placed between the substrate and the device layers. This view is to some measure responsible for the present low level of bulk crystal quality.

The substrate is not a passive segment of epitaxial device structures. It affects critically the yield of devices, their reliability, performance level, and life, primarily through structural and chemical contamination. Specifically, line defects (dislocations) in the substrate propagate into the epitaxial layers during their growth. Point defect clusters, inclusions, and second-phase microprecipitates nucleate corresponding defects in epitaxial structures. Fast-diffusing interstitial impurities can readily contaminate epitaxial layers during growth. Furthermore, heat generated during device operation leads to point defect diffusion, interaction, and clustering, which cause device failure. Compositional variation in the substrate can affect the lattice mismatch and result in misfit dislocations at the interface with the epitaxial layer.

Bulk Crystal Device Structures (Simulated Epitaxy)

All integrated circuit structures are fabricated on semi-insulating crystalline substrates. Circuits fabricated by ion implantation must be thermally annealed to remove implant damage. The electrical behavior of substrates following annealing depends on the stoichiometry and doping of the crystal.

GaAs can be made semi-insulating either by doping crystals during growth with a deep-level impurity, such as chromium (about $10^{16}/cm^3$),

or alternatively by the vapor pressure during growth that creates deep-level stoichiometric defects (EL2 centers). The latter technique is generally preferred, since these substrates are more stable against thermal conversion than doped substrates. The chemical and structural quality of the bulk crystals directly affects the device structures formed by implantation. Specifically, defects and chemical inhomogeneities decrease device yield, increase variations in the characteristics of individual devices, and decrease device life. It should be emphasized at this point that there is little current understanding of any of the defect-related processes occurring during thermal conversion, implant activation, and wafer annealing.

U.S. Competitive Position

The overall status of commercial compound semiconductor crystal growth in the United States is distressing. Japanese R&D efforts in this area greatly exceed U.S. efforts. There are some 15 U.S. commercial suppliers of GaAs, compared with about 11 in Japan. With the possible exception of one (MACOM), all suppliers in this country are small corporations with limited R&D facilities and efforts. Japanese companies are investing considerable resources in the development of improved crystals, and they currently have the major market share. There is only one small supplier (staffed by a few engineers) of InP in this country, while offshore commercial growers have a significantly larger InP production base.

A number of U.S. manufacturers seem to prefer Japanese wafers, apparently because of increased control of subtle differences in electrical properties and attention to details such as particular care in packaging of the wafers (e.g., polyethylene containers that do not flake or leave organic residues).

Several discoveries and innovations in bulk crystal growth have been made in the United States, but they remain as isolated advances, with their potential neither explored nor exploited. Among those advances one should include the improvement of crystal homogeneity by applying magnetic fields to the melt during crystal growth [Witt et al., 1970], the introduction of pyrolytic boron nitride (BN) as a crucible material, which eliminated contamination from the silica crucibles and led to undoped semi-insulating GaAs [Swiggard, 1978], the establishment of the relationship between stoichiometry and thermal stability of GaAs [Holmes et al., 1982; Ta et al., 1982; Parsey et al., 1982], and the identification of relationships among growth parameters, defect structure, and electronic characteristics [Gatos and Lagowski, 1983].

On the other hand, major technological advances in the growth of III-V compound single crystals for large-scale device fabrication have been made in Japan [Institute of Physics Conference Series, 1985]. These include the following:

- Shallow thermal gradient configurations, both in Czochralski and in Bridgman commercial installations. These were achieved by multiple thermal-zone furnaces and thermal-buffer systems. Shallow thermal gradients are critical in optimizing and controlling defect structure and chemical homogeneity.

- Total encapsulation in Czochralski growth. By maintaining the entire crystal under the boric oxide encapsulant, the arsenic loss during cooling is eliminated and thermal stresses during cooling are decreased.

- Arsenic vapor-pressure-controlled Czochralski growth. Here the encapsulant is eliminated, and the arsenic pressure over the melt is controlled by an arsenic source, as in the case of Bridgman growth. In this way, stoichiometry control is readily achieved and the disadvantages of encapsulation are eliminated.

- Growth in magnetic fields. Incorporation of magnetic fields in large-scale crystal growth has led to the essential elimination of twinning and related effects because magnetic fields apparently lead to a relatively planar interface. The commonly acknowledged advantages of magnetic fields relating to suppression of convective interference become of secondary importance.

- Vapor baffles. Especially designed baffles were developed and positioned over the melt and about the growing crystal in Czochralski facilities. They decrease substantially the loss of the volatile constituent. This approach has proved most important in the case of InP crystal growth.

CRYSTAL GROWTH IN MICROGRAVITY

The growth of crystals in space, where gravitational forces are considerably less than those on earth, provides an environment where mass transport in fluids is dominated by the diffusion of the constituents and not by convective flow as on earth. Inhomogeneities in crystal composition and dopant segregation should therefore be minimized in microgravity. In addition, the influence of the growth vessel on crystal growth, such as contamination, nucleation, and thermal conduction, can in principle be removed or altered, since it is no longer required to support the melt. Slip and dislocations induced at the growth temperature because of the mass of the crystal itself are eliminated in microgravity. Beginning with Skylab in the early 1970s, crystal growth in space has received considerable attention in the United States, Western Europe, and other countries, especially the Soviet Union. Ground-based experiments and theory have been performed, along with flight experiments on GaAs, GaSb, InSb, InSB-GaSb alloys, PbTe, SnTe-PbTe and GeSe-GeTe alloys, HgI_2, silicon, germanium, triglycine sulfate, and metals. It is reported that Soviet cosmonauts have performed approximately 100 GaAs experiments since 1978 using their "Kristall" furnace on Salyut 6,

although results have not been made available to Western crystal growers.

Many flights have produced unexpected results that have not yet been explained. This demonstrates the limitations of current understanding of gravitational effects on crystal growth. Nevertheless, a number of experiments have demonstrated the advantages of crystal growth in microgravity. These include the reduction of axial and radial composition variations, reduced contamination by the ampoule material, and several observations of improved crystallographic perfection. Convection is not entirely eliminated on the spacecraft due to residual forces from the spacecraft itself, as well as surface-driven convective flow. Theoretical modeling of the growth and careful measurement of all flows are essential components to obtain full understanding of crystal growth in space. The committee believes that considerable scientific benefit has already been derived from space experiments have produced definitive results.

Directional solidification work on GaAs, CdTe, HgCdTe, and PbSnTe alloys in space is being planned by several organizations involving NASA, university, and industrial research groups. The major limitation of microgravity research on crystal growth is the scarcity of flight opportunities. It is not possible to have a dynamic program based solely on microgravity when experiments are so few and far between. Available flight hardware is also a severely limiting factor. Inevitably, the major emphasis is placed on earth-based research. However, the few results that have been obtained have contributed significantly to understanding surface-tension-driven convective flow and heat transfer as well as fluid flow.

Space research on crystal growth does provide the opportunity to obtain improved understanding of crystal growth and to provide benchmark materials to guide future research on earth. While commercial exploitation of crystal growth in space is unlikely for cost-sensitive technologies in microelectronics, it is conceivable that the growth of unique crystals in space might be justifiable in the future. Future emphasis must be placed on more frequent flight opportunities and additional flight hardware if the potential of crystal growth in space is to be realized.

SUBSTRATE QUALITY

The parameters and requirements for the ideal substrate are very similar whether the material is silicon, GaAs, or CdTe. Stoichiometry, low or well-controlled impurity levels, surface finishing, and low defect density are some of the major concerns in substrate utilization. Stringent requirements in the substrate properties are essential for fabricating electronic and optoelectronic components.

The "Perfect" Substrate

The "perfect" compound semiconductor substrate would have properties that are not feasible today even for silicon. Among the needs are (a) uniform electrical properties such that dislocations, microscopic imperfections (including point defects), and macroscopic inhomogeneities such as impurity segregation, if present, do not modify device properties; (b) uniform stoichiometry for uniform activation of implanted layers; (c) surface flatness across the entire wafer of better than 0.5 micrometer with no bow or taper; (d) surface free from all types of polishing defects and extraneous particles; (e) uniform doping and background impurity concentration; and (f) mechanical strength such that wafer breakage does not occur in processing. Naturally, the ideal substrate does not exist, and properties are compromised in order to realistically manufacture devices at acceptable substate acquisition cost. Of the compound semiconductors, GaAs is probably the most advanced substrate material.

State-of-the-Art GaAs Substrates

The Table 4.1 lists some of the composite parameters taken from five different materials suppliers' data sheets for commercially available undoped semi-insulating GaAs substrates as of the beginning of 1987 [Mantech for Solid State Microwave Systems, 1985]. Substrates that match these properties are available from both domestic and foreign sources.

Current Practices in Substrate Preparation

Beyond the growth issues of producing large-diameter, thermally stable, semi-insulating GaAs boules discussed elsewhere in this report, there are additional important issues to the industry related to production and preparation of substrates.

One particular issue is that of slicing the boule. After proper orientation of LEC boules, the material is ground to the proper diameter, then orientation flats are milled. The boule is generally sliced with diamond saws to a slice thickness of about 0.838 mm (0.033 in.). Because of the thickness of the slicing blade, nearly one third of the boule is lost. Another major problem with current practice in slicing is the depth of saw damage from the process. This damage must be removed by lapping and polishing. Care must be given to subsurface damage that can affect electronic performance, but it is not readily apparent by surface observation.

The sliced wafers are then edge-rounded, lapped, mechanically polished, and chemically (hypochlorite or bromium-methanol solution) polished to remove the last traces of mechanical damage. During all of these processes, major problems include prevention of strain, breakage, and surface damage as well as maintaining cleanliness of the surfaces.

TABLE 4.1 Commercial GaAs substrate parameters

Diameter	76.2 mm (approximately 3 in.) ± 0.4 mm
Dislocations	Less than $10^5/cm^2$
Thermal conversion	No change in resistivity after 20 min. at 850°C
Resistivity	Greater than 10^7 ohm-cm
Thickness	0.635 mm (0.025 in.) ± 0.025 mm
Edge	Beveled or rounded
Bow and warp	Less than 15 micrometers total
Flatness	± 3 micrometers total over 76.2 mm (3 in.) dia.
Orientation accuracy	$\pm 1/4^o$
Surface finish	No haze or orange peel, no scratches or cracks, no foreign matter, no stains or fingerprints

Once foreign matter adheres to the surface, the wafer is difficult to clean, since the low damage threshold of GaAs prevents the use of strong mechanical action to remove particulates. The problem is even more severe in softer materials such as CdTe and HgCdTe. In addition, the insulating property of the 10^7 ohm-cm substrates creates a static charge that assists the foreign matter in adhering to the surface. Finally, special care is required in the polishing process to prevent bowing or warping. For example, the small wafer strain induced by holding the wafer during lapping can result in deleterious strain formation that is relieved by bowing when the wafer is removed from the lap. This problem is especially serious for the lithography of ultra-fine structures.

The issues related to the packaging and storage of GaAs wafers currently are not well defined. In general, there has not been either sufficient experience in handling large volumes of wafers or any degree of package standardization such as is found in silicon technology. The brittleness of the wafers requires that new or improved "gentle" equipment must be developed to allow cassette-to-cassette technology to be utilized reliably, an important issue if high-volume economy is to be realized. Many current wafers are hand-packaged in a vast variety of package formats. There are still major problems in achieving consistent wafers free of surface defects because of dust and strains.

The Japanese companies, with their larger volume use, appear to have spent considerable effort on packaging issues.

Quality Control of Substrates

Most substrate manufacturers perform their own first-order testing of their wafer material before sending out samples to the industry. However, there are no well-defined wafer tests that, if met, can guarantee acceptable device performance on all GaAs wafer production lines based on these wafer tests. Each user of the substrates generally performs in-house evaluation of the near-seed and near-tail wafers from a boule. If the in-house evaluation meets specifications, the user will buy the entire boule. Wafers rejected by one manufacturer may be subsequently procured by another manufacturer based on its particular processing technology. It is this uncertainty and variability in processes plus the absence of a "Caesar's wife" set of tests, which will guarantee that a given set of wafers is "above suspicion," that constitutes the biggest problem in the GaAs industry today--nonreproducibility. Quality control issues must be standardized with strong interaction between the processor and the supplier if the task of individual boule sampling and poorly controlled reproducibility are to be eliminated.

A major problem with many vendors of wafers is that they do not have all of the state-of-the-art analytical equipment necessary to fully characterize the wafers. Routine measurements such as Hall mobilities and resistivity are not truly standardized, especially when dealing with

high-resistivity material. The vast variety of needed characterization facilities range from x-ray through photoluminescence. Ideally, these should be performed over the entire wafer using imaging techniques. The average wafer vendor cannot afford this characterization, especially with the limited volume of sales and the increased competition. Methods of measurement of parameters such as bow, surface finish, etch-pit density, and implant activation are not well defined nor are there universally accepted standards. Some domestic suppliers have followed the lead of some foreign vendors in improving both packaging and characterization, but for many of the small companies the expense of such activities is prohibitive.

Material User Specifications

The problems experienced by the material vendor in trying to meet the needs of the user are exacerbated by the complicated specifications and lack of uniform standard processing set by the users. For example, implantation and epitaxial growth procedures are different for each user, and therefore the user's wafer acceptance requirements are different. Complicated specifications for wafer acceptance are employed by the user in an attempt to achieve reproducibility from its specialized processes. One company, for example, requires that the implantation activation efficiency shall be greater than 70 percent after implanting with a certain dose of silicon through a 900-nm film of SiN at 165 KeV. Another user wants an activation of at least 80 percent after a similar implant but does not specify a cap. In addition, both users specify different activation temperatures and times after implantation. A third user may not implant but grows an epitaxial layer on the material.

Another example in the nonuniformity of specifications is mobility. User A wants a value of greater than 4000 cm^2/V-sec, user B wants a value of greater than 4500 cm^2/V-sec after a post-annealing at 850°C, while user C wants a value of 5000 cm^2/V-sec. Some users have as many as 35 separate parameters that a wafer must meet in order to be qualified, including, in general terms, that the wafer is compatible with the user's processing line.

Meeting the user's specification and qualification tests, as well as the differences in the tests, places a very costly burden on both user and vendor. Since each user has unique specifications, the vendor generally falls back to supplying various users with sample material from the same boule, hoping that one of the users will find the material meets its qualifications. This lack of standardized substrate processes and acceptance specifications is currently being addressed by a Department of Defense manufacturing technology program. There is hope that a large number of these substrate procurement issues will be resolved in the near future.

The Role of Alternate Substrates

Considerable effort is currently devoted to the epitaxial growth of III-V semiconductors on silicon substrates [Posa, 1987]. The low cost, large size, mechanical strength, high thermal conductivity, and crystalline perfection of silicon substrates make such an approach attractive, especially in view of the possibility of integrating GaAs and silicon technologies. The lattice parameter of silicon is about 4 percent smaller than that of GaAs. This leads to a high density of misfit dislocations at the interface that propagate into the film. Several techniques involving buffer layers or strain-layer superlattices to accommodate the strain due to the mismatch have resulted in somewhat improved material quality. The thermal expansion mismatch of GaAs and silicon results in considerable bowing of the wafer upon cooling to room temperature, and the strained layer frequently cracks during processing. Nevertheless, both power and small signal transistors have been fabricated on GaAs on silicon and have exhibited performances comparable to equivalent devices on GaAs substrates. Whether large-area monolithic GaAs can be fabricated with acceptable yield and lifetime on silicon substrates is still an unproved issue. Beside the reliability issues, the R.F. loss of microwave lines on the relatively conductive silicon substrate (less than 10^3 ohm-cm for silicon versus greater than 10^7 ohm-cm for GaAs) may inhibit broad application for linear microwave circuits. At present, laser structures fabricated on this material have exhibited poor lifetimes [Kaliski et al., 1987], presumably because of defect motion during laser operation.

At this point, the structural quality of GaAs grown on silicon is considerably inferior to that grown on bulk GaAs substrates, and the future potential of this approach cannot yet be evaluated. Clearly the integration of optical and electrical devices on silicon is a strong motivation for further research. Efforts are in progress to grow InP and HgCdTe on silicon substrates, employing appropriate buffer layers or with GaAs as an intermediate layer.

Other Compound Semiconductor Substrates

The development of other compound semiconductor substrates, such as InP and CdTe, is lagging GaAs. The volume of such substrates produced is small, and the price is high. The primary use of InP is for light-emitting devices in the 1.3 to 1.55 micrometer region. The substrates also are used for potential millimeter-wave and microwave devices, but present use is very limited.

The far-infrared HgCdTe detectors require CdTe substrates; however, the ability to grow large-area CdTe or CdZnTe is very limited. The status of this technology is reviewed in Chapter 10.

Future Needs

There are substrate technology areas where resources must be directed to meet future user needs and to maintain a competitive domestic industry. At the onset, crystal-growth technology must be improved to give improved material quality and reproducibility. These techniques will likely require in situ intelligent control.

Although there is evidence that defects and nonuniformities of substrate materials affect the yield and performance of devices, the full effect of the substrate parameter cannot yet be evaluated without a full interactive program involving crystal growth, processing, and device performance. This is currently lacking. The largest-volume substrate suppliers achieve the greatest benefit from feedback regarding further substrate development; these are Japanese suppliers.

Silicon technology teaches that, as devices and processes become more sophisticated, the requirements on substrates become more demanding. For this reason, it is essential that substrate technology be developed in parallel with other device-manufacturing processes. Techniques for wafer-scale substrate characterization must be developed so that nonuniformities in substrates can be measured quantitatively and relationships between defects, electrical properties, and device performance can be established. A full understanding of the compound semiconductor substrates derived from such a study will allow establishment of a complete set of specifications that will remove the uncertainties associated with the effects of substrate variation on device yield.

Generally, there is a cost advantage for going to larger wafers and boules. Thus, the current 3-inch wafer will be replaced by 4-inch wafers and possibly even 5- or 6-inch wafers in the future. The use of larger wafers will require a heavy investment in equipment by the vendor. Another area is the use of cassette packaging and more automation in all the cutting, polishing, and characterization processes. The current cost of GaAs wafers is not likely to drop unless there is advancement in the use of automation in all wafer preparation steps.

Bulk crystal growth development is neither profitable (partly because of the low market volume) nor academically glamorous. It therefore requires a focused government-funded program to advance this technology. Current DOD-funded programs should be better coordinated to achieve maximum benefit. Justification exists for a center of excellence, as recommended in Chapter 2, where a joint industrial-university-government program could provide a common data base that is available to industry without costly, duplicative efforts. The necessary development cannot be justified by commercial markets alone. It also is desirable to encourage small-scale crystal growth efforts at universities to provide academic flexibility that is useful in identifying factors controlling the defect structures that dominate electronic characteristics.

Finally, alternative substrates, especially silicon, may play a major role in the future development of compound semiconductors. Device yield and reliability data are needed, and interfacial problems and material quality will have to be improved before a realistic assessment of this approach can be made.

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CHAPTER 5

MODELING OF BULK CRYSTAL GROWTH

PRINCIPAL RECOMMENDATIONS

Modeling is very useful both in understanding crystal growth phenomena and in improving apparatus design and the procedures for growing crystals. Intelligent control systems will require computer models. Unfortunately, such models often provide incorrect results because of incorrect assumptions used in developing the models, lack of data on physical properties, and failure to compare the predictions of the model with experimental data.

Recommendations for improving process modeling techniques include the following:

- Computer models should be compared with experimental results and modified until reasonable agreement is obtained.

- A major effort should be mounted to measure the physicochemical properties needed in developing computer models.

- Supercomputers should be used so that three-dimensional time-dependent problems can be solved.

MODELING BULK CRYSTAL GROWTH

In situ process control of compound semiconductor bulk crystal growth from the melt is complicated by the opaque character, high melting points, high vapor pressure, and toxicity of typical semiconductor melts. In situ experimental diagnostics are limited to measurements of surface temperature and of the meniscus shape at the crucible wall and at the melt-solid interface (when visible). Additional information available before or after growth can be obtained from temperature profiles within the melt and analysis of crystals for composition morphology and interface shape.

Modeling studies provide a vital link between the fundamental principles and experimental variables governing crystal growth and process engineering. In recent years, there has been considerable activity in modeling the macroscopic transport phenomena (heat, mass, and chemical

species) that characterize the growth of semiconductors from the melt. Some goals of these studies have been to (a) develop an understanding and explanation of experimental observations; (b) optimize hardware design; and (c) develop intelligent control systems. Progress has been made, using computer simulations of molecular dynamics at solid-fluid interfaces, in understanding micromorphology and growth kinetics. To date, modeling of the macroscopic variables has provided more insight into the important experimental variables necessary to improve and control crystal growth.

Three types of modeling have been employed--experimental analogues, analytical theories, and numerical computations. There are advantages and disadvantages of each. Experimental analogues are typically low-melting transparent materials, such as organic compounds or molten salts. Suspension of insoluble particles in the melt allows convection currents to be observed and velocities to be measured throughout the melt. This flow visualization provides valuable first-principles insight that cannot be obtained on semiconductor melts. Temperature measurements in the melt and the crystal are also easily obtained. Both the velocity and temperature measurements provide data for verification of computer models, which then can be applied to compound semiconductor growth.

The problem with these analogues is that their thermophysical properties are not the same as for semiconductors and hence provide little quantitative information. Semiconductors are distinguished by their low Prandtl numbers (low viscosity and high thermal diffusivity) and high melting points. The thermal conductivities of analogue materials are generally orders of magnitude lower and have much lower melting points and thermal gradients, so it is never clear how applicable the results really are to semiconductors, even in a qualitative way.

In theoretical modeling, the first step is typically a simplified analytical solution for a small problem, such as the first treatment of constitutional supercooling and the first theories for temperature gradients in a crystal during Czochralski growth. The advantage of such models is that they provide great physical insight and yield information on the functional dependence on the experimental variables and the physicochemical properties. The disadvantage is that they do not account for the complexities of real systems. In addition, implicit assumptions often are made that do not correspond to reality. For example, in theories for diffusion in multicomponent mixtures, it is often assumed that the diffusion rate of each component is proportional only to its own concentration gradient. (This is true only if the concentrations are all very small and the components do not interact with one another in any way.) The stagnant film model is often used for heat and mass transfer computations, even though the model is known to be fictional and to give erratic predictions, especially at high growth rates and for microscopic phenomena such as cellular or dendritic growth.

Numerical modeling with the computer makes it possible to take into account all the complexities and interactions of a real system, although it has been common practice to make simplifying assumptions to reduce programming complexity and computation time. Most applications have dealt with transport phenomena (fluid mechanics, heat and mass transfer) with which chemical and mechanical engineers have a great deal of experience. Transport phenomena determine compositional homogeneity, interface shape, morphological stability, etc. Recently, investigations have begun on thermal stresses, plastic deformation, and point defect behavior in the hot crystal between the time it forms and cools to room temperature. Such efforts are hampered by ignorance, not only of the physicochemical properties versus temperature, but often even of the basic phenomena operating in the solid while it cools.

Although numerical results are useful, it is easy to lose sight of their limitations, such as these:

- To gain insight, it is necessary to perform a complete parametric study. Even then, it is often difficult to make generalizations from the results.

- The boundary conditions selected do not always correspond to reality. For example, in analyzing convection in the vertical Bridgman-Stockbarger technique, it has been common to assume that the temperature in the heater is uniform. Although one can achieve nearly isothermal conditions with a heat pipe, it is more common for the temperature to vary significantly with height. This has a significant effect on both the magnitude and the patterns of the convection.

- Axisymmetric cylindrical symmetry is often assumed to guarantee computation of axisymmetric convection. Recent organic analog experiments with the vertical Bridgman geometry have rarely shown axisymmetric convection.

- Steady state is usually assumed, which provides no information on transients or on the stability of the solution.

- There is an absence of data for many or even most of the physical properties used, especially at high temperature. Examples are thermal conductivity, viscosity, dependence of surface tension on temperature, diffusion coefficients, solubilities, emissivities and optical absorption, and critical resolved shear stress versus temperature and composition. Not only are there few data for the physical properties of compound semiconductors, but also the high-temperature properties of the ampoule and furnace materials are frequently unknown.

- No comparison is made with laboratory experiments to refine ("verify") the model before it is used for computer "experiments" to test apparatus design concepts, different operating modes, and control algorithms.

Despite these limitations, considerable progress has been made in recent years, and the results have provided valuable insight into processing. The following are some examples:

- Computation of plastic deformation in GaAs caused by thermal stress during Czochralski growth. This has clearly demonstrated the importance of convection and thermal gradients in dislocation formation and distribution.

- Computation of growth rates and composition in diffusion-controlled liquid epitaxial growth of various compound semiconductors.

- Influence of magnetic fields on transport phenomena in Czochralski growth.

- Analysis of control strategies for Czochralski growth that consider both heat transfer and meniscus behavior. DOD-sponsored efforts for GaAs are currently under way at Arizona State University, General Electric, and Westinghouse.

- Influence of the pressure of inert gas on evaporation from a melt. It has been shown that this is an ineffective means for controlling evaporation.

- Analysis of heat transfer in HgCdTe solidification. The difficulties in obtaining a planar interface because of the variation of thermal conductivity with temperature have been demonstrated.

- Design of an after-heater and a bottom heater to reduce thermal stress in liquid-encapsulated Czochralski growth of GaAs.

The ultimate value of theoretical modeling lies in the ability to predict the effect of process variables on crystal growth and to provide detailed in situ control with the limited experimental data inputs available in real time. Molecular dynamics can provide understanding of nucleation events and defect formation on a molecular scale, whereas continuum modeling provides the macroscopic information on crystal uniformity, dopant incorporation, and strain distribution.

To realize this potential, further work is necessary to develop three-dimensional models that represent real crystal growth situations. A top priority is to have close interaction between experimental crystal growth and theoretical modeling that will provide appropriate specific experimental boundary conditions for theory and to test theoretical prediction with experiment. Only when the loop has been closed will real-time process control be feasible.

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CHAPTER 6

EPITAXY

PRINCIPAL RECOMMENDATIONS

Low-cost manufacturing of compound semiconductor devices requires high wafer uniformity, high yield, and high throughput epitaxial techniques. The majority of commercial devices are fabricated using liquid phase epitaxy (LPE) or vapor phase epitaxy (VPE). However, the most promising techniques for the growth of complex structures of the future are molecular beam epitaxy (MBE) and organometallic vapor phase epitaxy (OMVPE, MOVPE, OMCVD, MOCVD). The United States has been at the forefront, pioneering both of these approaches. However, this innovation has not established a clear lead in the development of equipment for manufacture. To meet the challenge of manufacturing reproducible and affordable compound semiconductor devices, concerted effort must be focused on the issues of scale-up, increased throughput, yield, and uniformity. This will be accomplished only by a close coupling of basic research into the chemistry and physics of the growth process with equipment design and engineering and with device fabrication. Since U.S. equipment manufacturers are not vertically integrated, semiconductor manufacturers have limited access to the knowledge base required for equipment development. A closer collaboration with university and industry must be established.

The early investment in basic material technology using MBE has been the inspiration of most quantum-well and two-dimensional electron gas concepts. More recently, OMVPE has overcome obstacles related to purity, and the ability to grow abrupt interfaces on an atomic scale, comparable to MBE, has now been demonstrated. The combination of the advantages of OMVPE with those of MBE now appears to be a particularly promising direction for scale-up and manufacturability. Such advances will be important for current technology and essential for future developments of new concepts that use artificially structured materials. The following research and development programs are specifically recommended:

- Conduct surface studies of crystal growth, including nucleation, surface kinetics, and the effects of interface strain and defect propagation.

- Initiate additional basic studies in OMVPE on chemical reactions involved in the deposition process.

- Conduct cooperative R&D efforts, which include domestic equipment manufacturers, on gas phase MBE, atomic layer epitaxy, and photon and plasma-assisted growth. The focus should include scale-up, multiple-wafer growth, automation, reproducibility, throughput, and system cost.

- Develop high-purity and low-toxicity organometallic sources.

- Model hydrodynamic, thermodynamic, and kinetic aspects of OMVPE growth for advanced equipment and process design.

- Develop real-time process control for crystal growth and in situ characterization techniques, particularly for OMVPE.

CRITICAL ROLE OF EPITAXY FOR NEXT-GENERATION DEVICES

During the past decade, device physics has undergone a revolution. Device performance has increased significantly for such devices as lasers, detectors, and transistors based on heterojunctions and superlattices with atomic dimensions [National Research Council, 1985]. For the fabrication of some of these compositionally modulated superlattices, it is necessary to switch repeatedly and reproducibly from one composition or doping level to another within a distance of 1 nm or less. In addition, the search for improved device performance has led to the need for a wide range of III-V semiconductors and alloys: AlGaAs-GaAs for lasers, light-emitting diodes, and transistors; GaInAsP-InP for lasers and detectors used in fiber optic communication systems and very-high-speed transistors; AlGaInP-GaAs for short-wavelength lasers for optical memory applications. Even more exotic alloys are in the research stage for future generations of devices.

Neither the special heterojunction and superlattice structures nor the alloys required for these structures can be fabricated in bulk material (i.e., material grown from the melt by Czochralski or Bridgman techniques). They require epitaxial growth techniques capable of growing ultrathin, single-crystalline layers with extremely high-purity and super-abrupt interfaces. They also require the versatility to handle the many materials systems in use today. For production applications, there is need for economy with good control, excellent uniformity, and excellent reproducibility. The requirements for current and future eptaxial systems can be stated in terms of the parameters listed above. The impurities contained in the epitaxial layers must be controlled to levels in the low $10^{14}/cm^3$ range, i.e., approximately 10 parts per billion. The interface abruptness must approach one atomic layer of about 0.3 nm.

In this chapter, mature epitaxial techniques such as liquid phase epitaxy and hydride and chloride vapor phase epitaxy are addressed briefly. While these techniques will continue to play important roles in manufacture, the emphasis of this chapter is placed on the more recently developed techniques of MBE and OMVPE as well as possible hybrids of the

two, designed to capture the strengths of each. These techniques offer capabilities that are better suited to the fabrication of the more complex device structures anticipated in the future. This chapter focuses on assessing the current state of the art, identifying key problems that limit the technology, identifying areas where breakthroughs might be realized, comparing the status of domestic versus foreign efforts, and, finally, making recommendations on which areas should receive either increased support or need a better overall strategy that could significantly enhance the development of the necessary manufacturing technology or produce breakthroughs in the technology.

LIQUID PHASE EPITAXY

LPE has been the dominant manufacturing technology to date for discrete optoelectronic devices. It has yielded the high-quality material required for simple laser and detector structures. The processing techniques have been refined to realize some of the more complex heterojunction structures required for high-performance devices.

LPE is a simple equilibrium-growth technique in which a solution containing the semiconductor constitutents is brought into contact with the substrate surface to initiate growth. Multilayer structures are grown by sequentially sliding melts of different composition over the substrate. Growth rates and thicknesses are controlled by controlling melt composition (according to the phase diagram) and by very precise control of melt and substrate temperatures. Even slight temperature transients during the growth process can produce major changes in solid composition and thickness. LPE apparatus has the advantage of very simple construction and low cost. It produces the highest purity III-V and II-VI compounds. Several review articles describe this technique [Dawson, 1972; Casey and Panish, 1978; Hsieh, 1980; Nakajima, 1985].

The primary shortcomings of LPE are the lack of large-area uniformity, poor surface morphology, graded (nonabrupt) interfaces, and inadequate layer-thickness control for the new generation of heterojunction and superlattice devices. Although there is little active research on LPE, it remains the major viable manufacturing technology for many of the simpler optoelectronic device structures. However, LPE will be displaced by OMVPE, MBE, or gas source MBE because they can produce the required quality of material with much greater uniformity and surface quality and the control needed for complex layered structures.

CHLORIDE AND HYDRIDE VAPOR PHASE EPITAXY

Two techniques involving the use of chlorine to transport the group III elements are both referred to as vapor phase epitaxy (VPE). The two techniques are best distinguished by considering the growth of GaAs

layers. In the chloride technique, Cl-VPE, the arsenic is introduced into the system as gaseous $AsCl_3$. This is passed over molten gallium that is held at a higher temperature, which reacts to form volatile GaCl and As_4. These are transported together to the GaAs substrate, which is at a lower temperature, and they react to form the epitaxial layer of GaAs.

In the hydride technique (H-VPE), the arsenic and chlorine are introduced separately, the former as volatile AsH_3, the latter as HCl, which is passed over the molten gallium to form GaCl. The AsH_3 pyrolyzes to As_4, and the reaction at the substrate is similar to that in the Cl-VPE case.

These two techniques were the first vapor phase epitaxial techniques developed for the growth of III-V semiconductors and are described fully in several review articles [Stringfellow, 1985a; Dorrity et al., 1985; Hollan and Hallais, 1982; Olsen, 1982]. Since the Cl-VPE techniques use a single, liquid source, which is easily purified, it produced the first extremely high-purity GaAs. The purity of the H-VPE material has been limited by the purity of the gaseous hydrides, which are known to contain water, oxygen, and GeH_4. Both techniques are highly developed and used in production operations. H-VPE is the process used for commercial GaInAs detectors and the large-scale production of GaAsP light-emitting diodes. Cl-VPE is used for the growth of high-purity GaAs for FETs.

The two techniques have several problems in common. Fundamental problems associated with the chloride chemistry prevent the growth of aluminum-containing compounds and alloys. This immediately eliminates these techniques for many interesting devices such as AlGaAs-GaAs lasers and high-electron-mobility transistors. The growth of antimony-containing alloys is also difficult. Versatility is not as great as OMVPE, since the substrate must be moved between different reaction chambers when changes in composition are required. In addition, the growth of abrupt interfaces is difficult.

A variation of the technique called vapor levitation epitaxy (VLE) has been developed recently [Cox et al., 1986]. It is so named because, during the growth process, the substrate is actually levitated by the growth vapors. The substrate wafer may be transported back and forth over different gas inlets for multilayer growth. It delivers excellent uniformity and good thickness control. Since it is compatible with the trichloride method, high-purity source material is not a problem, and its use for producing InGaAsP compounds has been demonstrated. Further development will be required if it is to be applied to other compounds. No commercial VLE equipment is available. Because of the problems noted for conventional VPE, chloride- and hydride-VPE techniques are being replaced by OMVPE and MBE for most applications.

ORGANOMETALLIC VAPOR PHASE EPITAXY

OMVPE is a vapor-phase epitaxial growth technique [Stringfellow, 1985b] where, in the purest form, the group III and the group V elements are transported using simple, volatile, organometallic molecules such as trimethylgallium (TMGa), trimethylindium (TMIn), trimethylarsine (TMAs), and tertbutylarsine (TBAs). The process is simple, with the organometallic molecules being transported from pure liquid or solid sources held in temperature-controlled bubblers into a controlled flow of high-purity hydrogen. The molecules are transported in the gas phase to the heated substrate, where they thermally decompose to form the desired III-V semiconducting solid. As will be discussed later, the apparent simplicity of the technique belies the complexities inherent in the actual growth chemistry and the hydrodynamics involved in gas flow and transport to the growing solid.

The development of OMVPE has progressed remarkably in the past few years from the technique originated by Manasevit [Manasevit, 1968; Manasevit and Simpson, 1969]. The early work was conducted at atmospheric pressure; in later years, however, low-pressure configurations have been developed that operate at pressures from approximately 76 torrs to as low as the 1- to 10-torr regime [Kamon et al., 1986]. Very recently, hybridization between the ultrahigh-vacuum MBE technique and OMVPE has resulted in operation at pressures below 10^{-9} torr [Tsang, 1986].

Versatility

Perhaps the strongest feature of the OMVPE technique is its versatility. It has now been demonstrated that the technique is capable of growing all common III-V compounds and ternary and quaternary alloys--i.e., those containing combinations of aluminum, gallium, and indium with phosphorus, arsenic, and antimony. Films are readily doped to produce both p- and n-types, and undoped GaAs can be grown to be semi-insulating by proper control of stoichiometry during growth. Another aspect of this versatility is the ability to grow these compounds on dissimilar substrates--e.g., GaAs on silicon. It also has the ability to grow selectively at low presure (1 to 10 torr).

OMVPE is capable of depositing semiconductor films on the exposed substrate with no growth on dielectric masks. This capability, useful for the fabrication of planar electronic and optoelectronic devices and the monolithic integration of these devices, is not possible at higher pressures in OMVPE but shows some promise by MBE [Okamoto and Ohata, 1987]. Another important aspect of versatility is the ability to grow at low temperatures, where dopants do not migrate and atomically thick superlattice structures are stable.

In the past, MBE has proved superior for low-temperature growth in comparison with the high temperatures required for the pyrolysis of the

group V sources, AsH_3 and PH_3. Recently, organometallic group V sources, such as tertiarybutylarsine (TBAs) and tertubutylphosphine (TBP) have been demonstrated to decompose at considerably lower temperatures (approximately 450°C) [Larsen et al., 1986; Chen et al., 1987].

It is most important to continue the development of organometallic arsenic and phosphorus sources for low-temperature growth. An alternative approach to low-temperature growth is to crack the organometallic compounds using light [Doi et al., 1986] or plasma-assisted decomposition [Pande and Seabaugh, 1984]. Photolysis offers the potential of selective growth only at illuminated areas. Reactor design is severely complicated by deposition on the windows that attenuate the optical beam. Plasma-enhanced OMVPE growth of GaAs also has been demonstrated at temperatures of 450°C [Pande and Seabaugh, 1984]. All of these low-temperature growth techniques are at an early research stage, but they could provide additional variables for the control of the deposition process.

Safety

A major issue now facing the epitaxial processers using AsH_3 and PH_3 is the danger associated with such highly toxic gases, especially when contained in high-pressure cylinders, where a single mistake could result in the release of large quantities of gas. Proper safety precautions are costly. Two choices are available to make the apparatus safe. One involves extensive precautions in equipment and facility design, sensitive toxic gas monitors, comprehensive scrubbing and ventilation systems, automated exhaust shutdown, and overall frequent process hazard reviews [Lum et al., 1986]. A second preferred alternative is to develop low-vapor-pressure liquid organometallic group V sources that allow the growth of high-purity III-V semiconductors with minimal risk and at a reasonable cost as substitutes for AsH_3 and PH_3. In addition to their much lower volatility, many of these sources are reportedly much less toxic. Previous studies of the growth of GaAs with alternate organometallic sources have shown significant carbon incorporation in the films, which is detrimental to the electronic properties. Recently, however, high-quality growth and low-carbon incorporation have been obtained with tertiarybutylarsine [Lum et al., 1987]. In view of the increasing restrictions on the transportation and storage of highly toxic gases, development of low-cost alternatives, or methods for in situ generation of AsH_3 within the reactor, must be considered urgent.

Purity

The purity levels obtained in III-V semiconductors, in particular GaAs, InP, and GaInAs grown by OMVPE, are equal or superior to results

obtained by any other technique. Low-temperature electron mobility is considered the standard test for the presence of ionized impurities. As an example of the purity of OMVPE grown material, several laboratories have produced InP by OMVPE at both 760 and 76 torr with electron mobilities at liquid nitrogen temperature of greater than 130,000 cm^2/Vs [Chen et al., 1986; DiForte-Poisson et al., 1985; Zhu et al., 1985]. This indicates InP to be purer than when produced by any other technique.

Mobilities obtained in GaAs and GaInAs grown by OMVPE are comparable to those obtained in material grown by MBE and other epitaxial growth techniques. This improvement was recently achieved as a result of the efforts of the suppliers of organometallic source materials to develop new, high-purity synthesis routes and improved purification procedures. The purity currently available in commercially available group III organometallic sources is sufficient for most devices. However, if the new group V organometallic sources are to replace AsH_3, significant effort will be required before acceptable purity levels are obtained.

Interface Abruptness

Until last year, MBE was considered inherently superior for the growth of atomically abrupt interfaces because of the complex hydrodynamic aspects of the gas flow in an OMVPE reactor, particularly at atmospheric pressure. Recently, workers at Sony in Japan [Ishibashi et al., 1985] have succeeded in growing atomically abrupt interfaces in the GaAs-AlGaAs system using atmospheric-pressure OMVPE. Layers have even been grown one atomic layer at a time [Kobayashi et al., 1986], a procedure that has great promise for the design of new crystals on a monolayer scale.

Even more recently, results at AT&T Bell Laboratories [Miller et al., 1986] and at the University of Utah [Wang et al., 1988] have demonstrated the ability to grow atomically abrupt interfaces in the GaInAs-InP system on the basis of results with quantum well photoluminescence. This is particularly impressive since both the group III and the group V elements must be switched simultaneously to avoid the growth of GaInAsP alloys at the interface. While these are not isolated examples, the achievement of good uniformity, sharp interfaces, and high purity simultaneously is by no means routine. This has been done only on single-wafer research systems not suitable for direct scale-up.

Another important way of evaluating interface abruptness is to examine results obtained in two-dimensional gas (2-DEG) structures. Again, MBE has been consistently in the lead in the contest to obtain the highest low-temperature mobilities, with peak values of greater than 2×10^6 cm^2/Vs [Hiyamizu et al., 1983] for the GaAs-AlGaAs system as compared with values of 500,000 cm^2/Vs [Mori et al., 1986] for OMVPE material. However, the transconductance of OMVPE-grown 2-DEG FET structures is similar to those grown by MBE [Takakuka et al., 1986].

Defects

Vapor-phase epitaxial processes normally occur on the group V-rich side of stoichiometry in the pressure-temperature-composition phase diagram. On the group III-rich side of stoichiometry, metal droplets are formed on the surface that lead to the growth of whisker-shaped crystals by the vapor-liquid-solid mechanism. This produces defects not seen in LPE-grown material, which is naturally grown on the III-rich side of stoichiometry. For example, the defect EL2, believed to be related to the As-antisite defect, is always seen in OMVPE-grown GaAs and never in material grown by LPE. The occurrence and effects of these stoichiometric defects are not well understood at present. The morphological defects observed on the surface of OMVPE-grown GaAs have not been as well studied and characterized as the so-called oval defects endemic to the MBE process. The available data indicate that fewer process-destructive defects are found in OMVPE-grown material than in that grown by conventional MBE.

Modeling of Vapor Growth

The uniformity in composition and thickness of semiconductor layers depends strongly on the flow dynamics, i.e., the heat and mass transfer conditions that prevail in the vapor growth reactors used. The transport dynamics in VPE reactors are among the most complex encountered in industrial systems, and theoretical modeling of the effects is still in the early stages. The large differences in molecular weight of the vapor constituents typically used lead to Soret (thermal) diffusion effects that make significant contributions to diffusive fluxes. These are carried in highly three-dimensional combinations of forced and buoyancy-driven convective flows that arise from the flow-through operation and the steep temperature gradients characteristic of most VPE processes.

Although it has become apparent that layer qualities and uniformity are often limited by traditional VPE conditions, little progress has been seen in the past 20 years in the understanding of the fluid dynamics of vapor growth systems. Early smoke-flow visualization experiments were erroneously interpreted as revealing a stagnant or boundary-layer flow about the substrates. Most modeling has since been based on such an assumed behavior. Furthermore, the significance of buoyancy-driven flows and Soret diffusion have been underestimated by most workers [Hess et al., 1985]. Hence, most modeling has provided little guidance in the design, upscaling, and optimization of VPE equipment and processes. Costly trial-and-error methods have been the standard approach.

Most recently, however, numerical computation [Wahl 1984; Moffat and Jensen, 1986] and holographic experiments [Giling, 1982] have shown that reasonably realistic modeling of VPE processes, although taxing current computational capability, is possible. These few efforts have already

provided new scaling laws that can give guidance for reactor design. A serious handicap to realistic flow modeling is the currently limited knowledge of the actual, homogeneous, and heterogeneous reactions responsible for the deposition process. Since buoyancy-driven flows are particularly sensitive to compositional (i.e., density) variations, realistic VPE modeling requires accurate information about the temperature-dependence of the species concentrations involved.

Producibility

The OMVPE technique is in the early stage of commercial use for large-scale production. Cambridge Instruments sells a reactor capable of simultaneously growing on thirty 2-in.-diameter substrates or twenty 3-in. wafers. However, uniformity remains a problem in these reactors, and the ability to grow atomically abrupt interfaces has not been demonstrated. These reactors are used commercially at Applied Solar Energy Corporation for the growth of AlGaAs-GaAs solar cell structures. The large wafer throughput makes OMVPE potentially ideal for production operations. A 1.5 percent thickness uniformity over a 3-in. wafer has been demonstrated only in small reactors. The solution will come through an improved understanding of the hydrodynamics and mass transport in such large-scale reactors. For example, Emcore Corporation is developing a machine capable of producing 1500 wafers per week using a wafer carrier that spins at high speed to maximize growth uniformity. Modeling computation will be necessary to design efficient reactors for the scale-up of OMVPE.

Control of the OMVPE process requires precise temperature control of the organometallic source bath temperatures ($\pm 0.1^{\circ}C$), the flow rates in all gas lines, and reasonable control of the substrate temperature $\pm 5^{\circ}C$). This is particulary important for alloys with mixing on the group V sublattice, such as GaInAsP. In general, the degree of control required for each of these parameters is within the specifications of commercially available equipment. The equipment market is fragmented, with no dominant player. All told, there are over 20 OMVPE manufacturers worldwide; about five or six are in the United States. Most manufacturers are quite small and not likely to devote substantial resources to equipment research and development. This is due in part to the poor understanding of gas flow patterns and reaction mechanisms. Good modeling of OMVPE reactor design is necessary for scale-up.

Future Directions in OMVPE

OMVPE produces high-quality compound semiconductor materials, even though there is little understanding of the actual growth mechanisms and reactions involved. It is not known to what extent the pyrolysis reactions occur homogeneously in the gas phase or heterogeneously on the solid surface. The nucleation and growth processes necessary to produce

atomically abrupt interfaces have not been studied. Kinetic data required for modeling of the growth process and reactor design are unavailable. Progress has been based largely on trial and error.

The agenda for future OMVPE research and development must include the synthesis, evaluation, and purification of new organometallic source materials; the investigation of growth using nonthermal energy sources; the growth of single layers and artificial crystals by atomic layer epitaxy; hybridization with MBE; and scale-up that will result in commercialy available equipment capable of ecoromically and reproducibly growing uniform multilayer structures. Every item on this list would benefit immensely from a more complete understanding of OMVPE chemistry.

Improved interactions between the disciplines of organometallic chemistry and OMVPE technology are necessary to produce optimum organometallic sources. In the past, OMVPE developers have used whatever sources were available from the chemical catalogs, with little thought of inventing and developing new sources uniquely suited for the epitaxial growth of compound semiconductor layers. This practice has dictated many of the growth conditions and, to some degree, the success achieved. This is particularly limiting in preparing HgCdTe alloys where the high pyrolysis temperatures of commercial tellurium sources have forced growth at temperatures where the mercury vapor pressure is too high. The development of new group V sources is required, both for increased safety and for lower-temperature growth of III-V alloys. Unfortunately, so little is known about the growth reactions occurring in OMVPE that the design of new source materials depends purely on post facto results of OMVPE-grown layers. So much flexibility exists for the organometallic chemist to design new source molecules that the development process would be speeded up tremendously if the requirements were understood better.

The development of photolysis and plasma-assisted growth is hindered by the fact that it is not known which bonds must be broken and at what stage in the growth reaction they must be broken. An understanding of the hydrodynamics involved in OMVPE is also absolutely necessary for the development of large-scale reactors. OMVPE has been done at reactor pressures from 760 torr (1 atmosphere) to 10^{-5} torr. Decisions relative to the optimum pressure range have been made based on the interface abruptness obtained, the range of materials that can be grown, and the purity obtained, with little or no input from fundamental understanding.

Efficient development of large-scale multiwafer OMVPE reactors and process control will require basic understanding of the steps involved in OMVPE growth.

MOLECULAR BEAM EPITAXY

MBE is a relatively simple, evaporative-growth process that has been extraordinarily successful in producing a wide variety of materials and

complex layer structures in the research laboratory [Cho and Arthur, 1975; Chang, 1980; Ploog, 1981; Dingle et al., 1985; Tsang, 1985]. To achieve the desired level of impurity control, a vacuum of about 10^{-11} torr is required, which is well within the capability of current high-vacuum technology. The sources of the constitutents for crystal growth are usually elements, heated in small ovens to reach the necessary vapor pressure and produce a flux of the desired element. Standard MBE uses resistively heated effusion cells, but for high-temperature materials such as silicon, germanium, dielectrics, and some metals, electron beam evaporation is used. The growth rate is determined by the temperature of the sources, and layer compositions are controlled by opening and closing shutters in front of each source in an appropriate sequence.

The ability of MBE, because of the ultrahigh vacuum (UHV), to incorporate surface analytical tools in the growth chamber was instrumental in identifying surface cleanliness and optimizing growth procedures, and, in general, it contributed greatly to the understanding of device physics and fabrication. Later it evolved into system designs in which growth and analysis take place in separate chambers. In the past few years, a new concept has emerged where modules made up of chambers and their pumping facility are connected together with UHV sample-transfer mechanisms. Each module forms a station where a special function is performed. Sample introduction, preparation, growth, analysis, and processing steps can occur in different locations in the system. This keeps the growth chamber under a constant condition so the growth sequence becomes highly reproducible. It also shortens the cycle time, as substrates can be prepared elsewhere in the system and are ready for growth once they are placed in the growth position. A shortcoming of conventional MBE is that critical parameters are not directly controlled in real time to provide the reproducibility, reliability, and automation required for manufacturing. The key to realizing a manufacturing technology will be to develop real-time feedback and control over these parameters. A second limitation is that, because the sources are line-of-sight, the system dimensions limit the growth area over which adequate uniformity of the layer thickness, doping, and composition can be achieved.

Control of Growth Parameters

There are many parameters that must be precisely controlled during MBE growth to achieve reproducible epitaxial structures. Growth rate is controlled by the temperature of the sources, whereas thickness is controlled by the ability to start and stop growth abruptly with shutters at a predetermined time. The growth rate has been varied from 0.01 to 10 micrometers/hour with 1 micrometer/hour being standard. (The 1-micrometer/hour rate corresponds to 1 monolayer of GaAs per second.) Thus, with shutter opening and closing times of 0.1 sec, growth can be stopped in much less than an atomic layer of material. Growth rate has

been typically determined from calibration runs. The problem for MBE is that, as source materials evaporate during the growth process, the surface area of the source changes and hence the flux changes, even at a constant source temperature.

Doping levels and composition can be maintained to better than ±1 percent by the set temperature and the control of the source ovens. Since the beam flux varies exponentially with temperature, control to ±0.2°C accuracy and ±0.1°C stability or better is absolutely critical. Calibration is complicated by the change in radiative thermal losses at the evaporant surface when the shutters are opened. Extremely precise control and calibration have recently allowed deposition of germanium and silicon layers with about a one-hundredth monolayer accuracy [Bevk et al., 1986], thereby permitting the design of superlattices and artifical crystals on the scale of the crystal unit cell.

From a manufacturing perspective, growth rate--and hence thickness--are inadequately controlled because there is no real-time direct measurement of the fluxes. Real-time flux measurement and feedback control is clearly necessary for the most precise deposition control. Composition and growth rate can be rapidly monitored with reflection high electron diffraction (RHEED) oscillations, but this technique appears to be unsuitable for automation or monitoring by unskilled operators. Furthermore, RHEED oscillations require a nonrotating substrate, which adversely affects uniformity, and dopant fluxes will still require calibration runs.

Deposition uniformity (thickness, composition, and doping) is controlled by the system geometry. With current solid-source MBE, ±1 percent of the absolute value for composition and doping are achieved over 3-in. wafers. As systems are scaled up for either larger or multiple wafers, the vacuum chamber becomes increasingly large, and uniformity is more difficult to achieve. The current technology is clearly adequate for research and development purposes, but multiple-wafer, manufacturing-type systems are not yet commercially available. A system with a capacity of three 3-in. or seven 2-in. wafers is being tested at Fujitsu in Japan [Saito et al., 1987] and is limited by source purity. Most systems are, however, limited by background carbon from the system. Despite the carbon impurity, this purity is adequate for virtually all electronic and optoelectronic devices currently being fabricated.

Interface smoothness and abruptness have been the strengths of MBE. There is still research activity on smoothness at the single-atomic layer level, but interface quality is more than adequate for any type of next-generation heterojunction device. There is, however, considerable concern with small, oval defects and their impact on small lithographic features of VLSI technology. It has been shown that oval defects do not result in device fatalities, but they can significantly affect lithography and metallization. The lowest density achieved is about $100/cm^2$, and for VLSI it needs to be reduced by an order of magnitude. The sources of

these defects are primarily the surface-cleaning process, handling inside the MBE system, and the gallium source. The problem of particle contamination during sample transfer inside the MBE machine has not been adequately addressed by the manufacturers. This problem gets worse during extended periods of service because of buildup of evaporated material. Improved performance in this area will be required to achieve VLSI standards for MBE.

Materials Systems

Group III-V compounds have served as the development ground for MBE. The initial work of Cho and Arthur was done on GaAs, and most of the equipment has been developed using III-V compounds as the central goal. Binary, ternary, and quaternary alloys of gallium, indium, and aluminum with arsenic and antimony all have been successfully grown by MBE. Phosphorus compounds have not generally been successful by conventional solid-source MBE because of problems in controlling the phosphorus flux. The use of gas sources has largely solved this problem. Both n- and p-type dopants are readily available and are well controlled for all of the III-V compound alloys.

Excellent device results have been achieved with all of the wider-bandgap III-V alloys. The only systems that are not readily grown by MBE are InSb and antimony-rich InAsSb alloys. The problems here are a very low growth temperature and the inability to get extremely clean surface conditions before the initiation of growth. Extremely low growth rates are required. Recently, it appears that better results have been achieved by heteroepitaxy of antimonides on GaAs or silicon, in spite of the severe lattice mismatch, because of the well-developed surface-cleaning techniques for these materials. Since these narrow-gap semiconductors are largely used for infrared imaging arrays that require substantial electronic signal processing, monolithic integration with GaAs or silicon could prove to be a very substantial advantage.

GaAs-Si is a prototype lattice-mismatch, thermal-mismatch, and polar-on-nonpolar semiconductor system. It contains all of the elements that suggest problems in heteroepitaxial growth. However, it represents an important approach for a potential technological breakthrough in the monolithic integration or merger of previous disparate semiconductor technologies. The results of GaAs-Si research to date have been strikingly successful [Harris et al., 1987]. A number of GaAs devices and simple structures have been integrated with silicon devices and a 1K GaAs-Si SRAM has been demonstrated [Shichijo et al., 1986]. The real question now is that of dislocation control, the role of dislocations on the properties of devices, and the effect of thermal strain on device processing and lifetime. It appears that, for majority-carrier devices (FETs, MODFETs, etc.), the GaAs-Si device results are almost indistinguishable from conventional GaAs epitaxial structures [Shaw,

1987]. Bipolar devices represent a greater challenge, and a number of attempts to make lasers have been significantly less successful than conventional GaAs epitaxy approaches [Schichijo et al., 1986]. Recently, the first continuous-wave room-temperature laser has been reported, but with a threshold current four times larger than that of comparable GaAs devices and with an extremely short lifetime [Deppe et al., 1987].

Future Directions in MBE

Molecular beam epitaxy is still in a rapid state of development, yet it has produced a number of exciting device and IC results that are creating the need for MBE manufacturing technology. The key issues for a manufacturing technology are automation, scale-up, reproducibility, reliability, throughput, cost, and elimination of surface defects. These issues must be addressed in a combined effort involving both MBE users and equipment manufacturers.

In the applications area, there are potential breakthroughs for new materials, artificially structured materials, and in situ and maskless processing for three-dimensional devices and new electronic and optoelectronic ICs. The SiGe alloy system is one of recent investigation and exciting potential. Currently, there are investigations into using smaller-bandgap SiGe alloys as the base region in heterojunction bipolar transistors, as the conducting channel in modulation-doped FETs, and as infrared detectors [Bean, 1987]. Recently, efforts have been directed to the modification of the band structure of silicon for optical applications by creating superlattices having a period comparable to or smaller than the silicon unit cell [People, 1987]. Significantly more research will be required to assess the viability of these structures. The importance of this work is that it makes the powerful heterojunction device design alternatives applicable to silicon.

MBE provides the potential to deposit materials atomic layer by atomic layer and thus build up coherent layered structures in a nonequilibrium fashion. Alloys of AlGaAs, for instance, can be simulated by alternate layers of AlAs and GaAs, where the relative thickness of each binary semiconductor is adjusted to give the desired alloy composition. There is relatively little known about the detailed electronic and optical properties of these materials as they change from an ordered alloy at the atomic-layer level to a multiple quantum-well structure. The multiple quantum-well regime (alternate layer thicknesses of more than 10 nm) is well studied and now is used in numerous device structures. This is an area where unexpected phenomena could be obtained that will be important to advanced electron device structures.

So far, the efforts in artificially structured materials have focused primarily on one dimension because of the layering technology with MBE and OMVPE. However, as e-beam lithography and x-ray lithography technologies advance, the ability to create two- and three-dimensional structures on a

quantum scale is rapidly approaching. Because the density of states in solids changes dramatically in going from three-dimensional to two- or one-dimensional structures, optical absorption, emission, and tunneling resonances are expected to be much sharper. The interactions between reduced-dimensional electrons and holes and the physical lattice are also unknown. Reports that the ever-problematic surface Fermi-level pinning in GaAs is appreciably altered in quantum dots [Reed et al., 1986; Cibert et al., 1986] indicate that there will be unpredicted phenomena created in these reduced-dimension, artifically structured materials. These structures and new phenomena could be important for future generations of electronic and optoelectronic devices.

The technology of layered structures and artificially structured materials has been applied largely to group III-V semiconductors, but considerable efforts are now under way in group IV and II-VI semiconductors and metals. Eventually these techniques will be used to design composite materials with specific properties in areas of wide-gap optical materials, high-temperature superconductors, and magnetic materials.

GAS-SOURCE MBE (CHEMICAL BEAM EPITAXY)

A recent development in epitaxial technology combines the advantages of both MBE and OMVPE. It employs gas sources (hydride and metalorganic) in an otherwise standard MBE growth chamber. Depending on the degree of hybridization of the MBE and OMVPE techniques, this new process is variously called gas-source MBE (GSMBE), chemical beam epitaxy (CBE), or metalorganic MBE (MOMBE). Results demonstrated thus far have been truly impressive in fabricating closely lattice-matched layers, extremely abrupt interfaces, and high-quality quantum-well structures [Panish, 1987; Tsang, 1987].

In place of solid source materials to generate molecular beams in effusion cells, growth gases are admitted into the system through heated gas source crackers. Outside the system, a gas-handling system, similar to that in OMVPE, is used to control gas flows with precision mass flow controllers. For a system pressure below about 10^{-5} torr, the beam nature of the growth fluxes is maintained so that complex flow patterns encountered in OMVPE are avoided. A major impact on the MBE design, other than source delivery system, is the pumping scheme. Because of the high gas load, turbo and diffusion pumps (or cryopumps) have been used. The same care must be exercised in the handling and disposal of toxic materials as with conventional OMVPE.

This technique appears to have great promise for production. The capability to grow all combinations of III-V compounds and graded and multiple composition structures is clearly better with a gas-source system. Sources are not depleted during growth and can be changed without breaking vacuum. Monitoring gas flows (and hence flux) can be done

directly, and the possibility of introducing all constituents through the same gas manifold (thus eliminating substrate rotation) can have significant impact on manufacturing cost and reproducibility issues.

GROWTH-RELATED DIAGNOSTICS

In a manufacturing environment, automatic control of the process is essential. In situ monitoring is necessary to make diagnosis, to optimize processes, and to perform trouble-shooting. Because of its vacuum compatibility, MBE is well suited to incorporating a variety of analytical and diagnostic tools.

In MBE reactors, the growth and effusion cell temperatures, beam flux, deposition rate, and material composition are frequently monitored and calibrated. Mass spectrometers and ion gauges are used to detect background contamination and measure beam flux ratios. The growth temperature is measured by thermocouple, pyrometer, or other optical means. A newly developed atomic emission sensing technique has demonstrated superior performance in electron-beam evaporator-based MBE. Thickness control as low as 0.02 monolayer has been reported [Bevk et al., 1986].

Various surface analysis techniques have been used in conjunction with MBE to analyze both the structural and chemical properties of the material before, during, and after growth. These techniques, which include Auger, ESCA, and SIMS, should not be used inside the reactor because of the potential contamination, but they could be housed in a separate analysis chamber as part of the system. Although they are extremely useful during the R&D phase, none is necessary in a production environment.

One of the most useful in situ surface techniques is reflection high electron diffraction (RHEED). Originally employed to study surface cleanliness and verify epitaxy quality, it also is useful for substrate temperature and growth-rate calibration. The observation of RHEED intensity oscillations has proved to be the most accurate direct growth-rate monitoring method, even for submonolayer growth. It also provides surface composition information. In OMVPE systems, the growth temperature is monitored as in MBE, and gas flows are monitored by mass flow controllers. Other in situ concepts for monitoring growth are just beginning to be explored. Mass spectrometers are incorporated to study reaction products, and optical techniques such as ellipsometry and Raman scattering appear promising. Holographic interferometry can give information on gas flows. In MBE growth of $Hg_{1-x}Cd_xTe$, where the composition x must be controlled precisely for infrared detection, an automated ellipsometer with a rotating polarizer has been used to control composition at $x = 0.2$ to $\pm$ 1 percent.

IN SITU PROCESSING

One of the keys of silicon integrated circuit technology is the alternating and successive lithography, diffusion, epitaxial growth, oxidation, metallization, and etching steps that are done to build up an extremely complex, multilayer integrated circuit. There is currently no reliable restart capability for MBE growth. Thus, most complex MBE structures are grown in a single-epitaxial, multilayer-growth process, with subsequent processing from the topside to define contact or to provide limits to different layers in the processing steps such as metallization and insulator deposition; this can be done in situ in the controlled UHV environment to prepare atomically clean interfaces. Localized lithography and patterning could be done during the growth process using laser, plasma, and reactive ion etching or with focused ion-beam direct-write methods. Although it is still an open question whether such methods will pay off, they provide another dimension for the fabrication of ultra-small, three-dimensional device structures. The controlled environment reduces the need for very expensive clean-room facilities and, with automated process control, should result in much-improved device yield.

CRITICAL PRODUCTION ISSUES

Both OMVPE and MBE have been used for small-scale production. Currently, MBE pilot lines produce about fifty 3-in. wafers per week, but this can be readily increased several-fold. By carefully calibrating temperatures and fluxes, less than 3 percent wafer-to-wafer variation can be attained. Shutters, temperatures, and the growth sequence are computer-controlled. In the best case, continuous operation in excess of 500 hours has been demonstrated. Routine, reliable long-term operation has not been demonstrated, however.

Sample exchange is currently accomplished through a vacuum load lock. Systems with three chambers achieve excellent vacuum isolation and reliable sample exchange. The major problem is that this is currently entirely a manual operation, and most of the current technology does not appear amenable to computer control and automation. While this is adequate for pilot-line operations, an entirely different approach needs to be developed for full-scale manufacture. Thin-layer structures, such as the MODFET, require growth times of approximately 10 minutes, and the throughput of current MBE systems is dominated by the sample exchange process.

Although throughput in OMVPE is potentially large, to get the necessary uniformity and interface control, capacity is limited at present to one or two wafers per run. Wafer turn-around is slow but can be improved with the addition of a sample loadlock mechanism. Significant progress has been made in recent years on system reliability and reproducibility. Wafer capacity has increased and the cost per unit-wafer

area for epitaxy has decreased dramatically, an encouraging trend. At present, epitaxy adds about $200 to the wafer cost. For small discrete devices, this is quite acceptable because of the large number of devices per wafer. Yet, to make larger-scale compound semiconductor circuits and devices truly affordable, this expense must be reduced considerably. A hundredfold increase in wafer throughput is needed--a goal that should be attainable by increasing the growth area, growth rate, and system efficiency.

Some combination of OMVPE and MBE offers the best potential for scale-up. Such a system will be a formidable challenge, and several critical equipment and process technologies must be developed and demonstrated, involving the following:

- Beam source design to provide high uniformity over large area
- Uniform doping methods
- New in situ monitoring techniques
- Sophisticated gas flow control and in-line purifier
- Pumping system suitable for a heavy gas load while maintaining system cleanliness
- Growth gas purity and safety
- Increased growth rate, possibly aided by energy-enhanced techniques such as photon or ion excitation
- Complex wafer platen transport system
- Automated process control
- In situ processing techniques

COMPETITIVE POSITION

A decade ago, the United States led in all areas of MBE and MOCVD. MBE was invented and most extensively developed domestically in the late 1960s and 1970s [National Research Council, 1985; Dawson, 1972]. During this period, four companies developed MBE equipment capabilities: Varian Associates and Perkin-Elmer Physical Electronics in the United States and Vacuum Generators and Riber ISA in Europe. During this time, ANELVA and Ulvac in Japan also built a few systems; however, neither was a significant factor in this development period, even in Japan. The picture began to change significantly about 1982. During the past 5 years, the numbers of installed MBE systems and personnel devoted to this technology have increased far more rapidly in Japan than in Europe or the United

States. Compared to the United States, the Japanese are certainly on par or ahead in efforts today. The area of greatest concern is their emerging equipment development. The first large, prototype manufacturing system, involving simultaneous growth on three 3-in. or seven 2-in. wafers, has been developed at Fujitsu with MITI support [Saito et al., 1987]. The system design has been done by Fujitsu, with much of the fabrication done by Eiko Engineering, a company previously unknown for its MBE technology. ANELVA and NTT have entered into a similar close relationship to develop a production MBE capability.

The United States currently retains a lead in gas-phase MBE research, but France and England already have a dominant position in this new market.

Much, if not most, of the recent breakthroughs in OMVPE have occurred in Japan. A brief list of areas in which Japan holds a clear technological lead include photon-assisted OMVPE, selective epitaxy, short-wavelength (red, yellow) injection lasers, and 2-DEG devices. Sony Corporation is using atmospheric-pressure OMVPE for the production of 0.86-micrometer lasers for compact disc players, optical memory devices, and 2-DEG transistors. European firms appear to have an initial lead in the use of OMVPE for the production of HgCdTe for IR detectors and lasers for fiber optic systems operating in the 1.3 to 1.6 micrometer range.

The United States has been unable to capitalize on its initial research lead for implementing the transition of this work to development and manufacture. Thus far, Japanese equipment manufacturers have not pursued sales aggressively outside of Japan, so the United States can still prevent monopolization of manufacturing technology by the Japanese. It will, however, take investment in the equipment sector and collaboration between instrument manufacturers and device manufacturers to avoid future overseas dependence.

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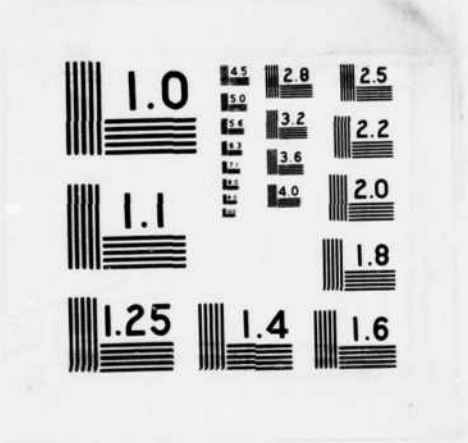
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CHAPTER 7

ETCHING AND LITHOGRAPHY

PRINCIPAL RECOMMENDATIONS

Many applications of compound semiconductors impose unique requirements on the etching processes used to pattern the wafer surfaces. Etching processes for each application have generally been developed independently of each other, and no generic etching technology suitable for all optical and electronic devices has yet emerged. Wet chemical etching is still used extensively with considerable success, but several limitations of wet etching for future technology are evident. These include inadequate etch rate control and uniformity, poor in situ monitoring techniques, difficulties with lift-off when thick gold metallization is used, and inadequate anisotropy for fine-line lithography.

To overcome these problems, a variety of plasma and reactive ion etching techniques, commonly used in silicon processing, are being extensively developed for compound semiconductors. However, the different reactivity and volatility of the group III and group V elements can lead to gross departures from stoichiometry on the semiconductor surfaces. High-energy ion bombardment causes surface damage, and plasma etching generally results in roughened surfaces. These issues must be overcome if plasma etching (with the associated benefits of in situ control) is to replace wet chemical etching. Microwave plasma etching with lower partial energies and ion-beam-assisted etching solve some of the current problems, but no single solution for all problems associated with group III-V etching has yet emerged. A solution of these problems will require more detailed understanding of the fundamental etching mechanisms, the causes of roughening, and the nature of the surface damage.

The trend toward higher-density and faster circuits requires new lithographic processes for high-resolution patterning of semiconductor wafers. Conventional optical lithography has about 0.7 micrometer resolution, and reduction to about 0.3 micrometer appears feasible using short-wavelength ultraviolet light. For dimensions down to 0.1 micrometer, direct electron-beam writing can be used for low-volume niche applications. However, for high-throughput projection, x-ray or projection ion-beam techniques will have to be developed further. This technology is driven by silicon technology and can be directly transferred to compound semiconductor technology. However, the manufacturing of

lithographic equipment will need more emphasis and support if the United States is to have a competitive position.

To achieve the required goals in etching and lithography, the following recommendations are presented:

- Conduct basic research in fundamental processes in plasma etching--studies of surface reaction, damage mechanisms, and plasma chemistry.

- Develop in situ diagnostics of the plasma, the etch rate, and the uniformity.

- Establish close interaction between equipment manufacturers and device processers to develop a viable manufacturing etching technology.

- Apply new x-ray and ion-beam lithography techniques, currently under development for silicon technology, to compound semiconductor technology.

ETCHING

The ability to pattern structures on compound semiconductor surfaces and on overlaying dielectric or conductive films is an essential step in the fabrication of all compound semiconductor devices. Etching may be used to remove entire layers, such as removing surface damage from semiconductor wafers or stripping photoresist off the wafer surface. Alternatively, etching may be used to selectively remove semiconductor material exposed through lithographically formed masks.

For macroscopic features, such as holes in the entire wafer for through-chip interconnection and chip separation, fast, selective, and anisotropic etching is required. For optical devices, optically-smooth surfaces with well-controlled etch profiles are required. For LSI or VLSI electronic devices, minimum surface damage and high anisotropy are necessary. To date, techniques for each application have been developed independently, using different approaches. Little attention has been paid to generic approaches to etching that are suitable for integration of optical and electrical components on the same chip. In the near future, the technology will consist of a variety of wet and dry etching techniques that optimize the available characteristics of each.

Wet Etching

In silicon technology, etching is almost exclusively done by plasma etching. While plasma etching of compound semiconductors is gaining ground, particularly for electronic devices, wet chemical etching is still

extensively used for device fabrication. Wafers are immersed in a solution such as bromine-methanol to dissolve away the exposed regions of compound semiconductors. The resulting newly exposed material is clean and undamaged, and, with available etchants, the stoichiometry is determined by the solid composition and not the etchant. A limitation of wet etching, particularly when feature sizes become very small, is undercutting--that is, dissolving material underneath the mask. Some etchants are highly crystallographically selective and suitable for fabrication of devices when only one, or a few, crystallographic facets are etched. The v-groove etched into the substrate of a CSBH laser shown in Figure 3.5a is an example of such etching. Etching ceases (or greatly slows down) when the <100> facet is dissolved and only <111> facets are exposed. Etchants of this kind (superoxol or H_2SO_4) can be used to form etched mirrors of integrated lasers and detectors. Crystallographically sensitive etching is a very limiting factor for preparing higher density electronic device structures. An additional difficulty with wet etching is that etch rate control may not be good enough for future devices, particularly over large areas. Edges tend to etch faster because of the nonuniform depletion of reactants near the semiconductor surface. End-point detection and in situ depth monitoring are complicated with wet etching techniques.

GaAs integrated circuit technology has relied heavily on gold-based metallization in high-speed circuits. Lift-off techniques using wet etching become increasingly difficult with the increasing thickness of metallization that is required in high-power circuits. Because of these factors, there has been considerable effort devoted to the development of plasma and ion-beam etching techniques for manufacture of compound semiconductors. In addition, more emphasis has recently been placed on the use of aluminum-based metallization in place of gold because of the diffculties encountered with etching the gold (see Chapter 9).

RF Plasma Etching

Dry etching by RF plasmas has shown considerable progress and has been the focus of extensive equipment development. The technique has been successfully used to produce highly anisotropic features in both the GaAs-GaAlAs and InGaAsP-InP materials systems [Burton et al., 1984]. In this process, the masked wafer is immersed in a plasma containing a reactive species such as chlorine or hydrogen atoms at pressures of 10^{-2} torr. The surface is bombarded by ions from the RF plasma with energies up to 1 keV, and surface atoms are removed at an enhanced rate by a combination of sputtering and the formation of volatile chemical compounds. Reactive etching of semiconductors is considerably faster and more versatile than sputtering by ion milling alone. For nonreactive metals such as gold, there is no improvement over ion milling, so lift-off technology is commonly used.

Anisotropy is achieved by exposure of the wafer to ion bombardment at appropriate angles. Additional crystallographic anisotropy may occur as with wet chemical etching, but this is often undesirable. Line-width control and profile shaping can be achieved using techniques such as sidewall passivation. High selectivity to photoresist and other films can be achieved by adjusting the reaction with multiple-step processing. Control over ion energies can be improved by adjusting the pressure and RF frequency. More recently, triode and magnetron systems have been introduced that give a greater degree of independent control over ion-flux energy. Throughput for commercial systems averages 20 to 40 wafers/hour, depending on the process. Automated cassette-to-cassette transfer of compound semiconductor wafers without breakage is now possible, as are computer control and data logging. Low particulate specifications (below $0.05/cm^2$) can be maintained in production environments. This market is still dominated by U.S. vendors, although equipment manufacturers in Japan have been gaining ground.

Compound semiconductor processing now increasingly makes use of dry etching systems, both for substrate etching and patterning deposited films. Two issues--sensitivity to damage by ion bombardment and unique contact technology--present problems that have not yet been solved using techniques developed for silicon technology. To a large extent, however, the etching of upper-layer films (dielectrics, metals, and photoresists) can directly adopt procedures used in silicon technology.

In contrast to silicon, which can be etched with either chlorine- or fluorine-based plasmas, the chemistry of reactive-ion etching of compound semiconductors is considerably more complicated. Although group V elements form volatile halides, group III halides tend to be nonvolatile, especially the fluorides [Flamm and Donnelly, 1981]. Group III chlorides are more volatile but have limited usefulness because the etch rates of the different semiconductor constituents in III-V alloys such as GaAlAs can vary widely. This variation results in a marked departure from stoichiometry of the surface region. Elevating the substrate temperatures to increase the reactivity and vapor pressure can result in improved stoichiometry, since the reactant flux becomes the rate-limiting factor.

Plasma etching of group III-V compounds generally results in surface roughening [Coldren and Rentschler, 1981]. While the origin of roughening has not been conclusively identified, it is often associated with nonvolatile reaction products or oxides. To achieve the etching of the optically flat surfaces that are necessary for integrated optics, this problem must be solved. Stoichiometry problems and the damage created by ion bombardment can result in serious degradation of the surface material properties. The surface damage problem remains a major obstacle to plasma etching of compound semiconductors. Typically, chlorine-containing plasmas, such as CCl_4, PCl_3, or HCl, are found to be adequate for GaAs. These gases make equipment corrosion problems more severe and limit the chemistry available for sidewall passivation. The addition of fluorine, such as CCl_2F_2, provides an effective stop etch at GaAlAs

layers. Exposing GaAs to hydrogen plasmas has helped passivate electrically active defects below the GaAs surface. Alternatively, surface damage can be reduced or eliminated by subsequent wet etching or annealing steps, but this is possible only in some limited specific situations.

Selective etching of dielectrics on GaAs is easy to achieve with fluorine-based plasmas. Deposited nitrides and oxides can generally be etched by the same techniques used in silicon technology, although the poor thermal conductivity of GaAs requires limited etch rates to avoid overheating the photoresist. Ion bombardment damage remains a problem.

Because gold-based alloys cannot be dry-etched successfully, alternative contacts using Al-Ge eutectic alloys [G. Troeger, personal communication, 1987] or refractory metals are under investigation. As these alternative contacts become more common, dry etching will replace lift-off technology for contact patterning.

A critical issue in Schottky barrier technology is recessing the GaAs surface to provide a good contact interface. This is presently accomplished with a wet etch consisting of an alkaline solution with hydrogen peroxide. However, the control and uniformity of this process limits yield. Thus, there is a need for a dry etch, which does not produce leaky Schottky barriers due to surface damage. This is at present the most critical etching need in compound semiconductor electronic technology.

In all three applications--etching substrate, dielectrics, and metals--dry etching is vitally important for compound semiconductor processing, and it will replace wet etching. Ion bombardment damage remains a serious issue, and equipment modifications will be needed to reduce the ion energy. Common RF plasma etching equipment requires operating at relatively high pressures (300 micrometers) and low power. End-point detection is commonly done using optical techniques such as plasma-emission spectroscopy and interferomety. Commercial systems are available, but selecting a good emission line to monitor the process can sometimes be difficult. Laser-induced fluorescence is emerging as an alternative technique because it is possible to select a particular species to excite. Diode-array end-point detection systems are beginning to appear on the market. They have the ability to monitor simultaneously up to 256 different emission lines, thus allowing for real-time in situ diagnostics of the plasma process.

Microwave Plasma Etching

The need to reduce damage from intense high-energy ion bombardment will become more critical for future submicrometer-size structures with shallower junctions. An emerging approach is to use 2.45-GHz microwave energy to excite a magnetically-confined plasma [Wertheimer, 1985; Sakudo

et al., 1977; Suzuki et al., 1977; Matsuo and Adachi, 1982]. Near-resonant coupling of the energy to the electrons creates a plasma with characteristics different from those of an RF plasma. Specifically, a very dense plasma can be maintained at low pressures (10^{-4} torr) and a much higher density of reactive radicals is excited.

Because of the high density of reactive species, high etch rates can be achieved with the wafer downstream from the microwave plasma. This essentially eliminates damage (and anisotropy) caused by the kinetic energy of the ions and is used (with oxygen plasmas) for applications such as resist stripping. Two U.S. companies fabricate downstream microwave plasma etching equipment. A microwave plasma etching approach extensively developed in Japan extracts ions from the plasma with a divergent magnetic field and focuses the ions onto the wafer surface with energies as low as 10 to 50 eV. This eliminates the need for an intervening grid and the associated problem of contaminants sputtered from the chamber walls and electrode structure. It also greatly reduces the potential for damage problems compared with RF plasmas. NTT and Hitachi in Japan independently introduced microwave etch (and deposition) systems several years ago. By 1987, microwave etching systems were offered by Anelva, Hitachi, Sumitomo, Tokuda, and the Semiconductor Energy Laboratory. No manufacturer in the United States or Europe yet produces a system of this kind. There is also no consensus that microwave-plasma etching is indeed superior to RF plasma etching as far as device performance and yield are concerned.

Ion-Beam-Assisted Etching

An alternative to either RF-plasma or microwave-plasma etching is to introduce an energetic argon ion beam into the etching gas [Barker et al., 1982]. While the increased ion bombardment gives rise to increased surface damage, control of ion flux and energy (typically 100 V to 2 kV) is quite flexible, and anisotropy and selectivity can be optimized. For instance, surface stoichiometry can be returned to the bulk values by using energetic ion bombardment to stimulate the reaction and desorption of both anion and cation products. Some limited equipment is on the market for ion-beam-assisted etching (e.g., the Technics RIB-160 and RIB-250 manufactured in Europe, or Veeco's Microtech and the Commonwealth Scientific 110 manufactured in the United States). This technique is currently being used to pattern Au-Ge-Ni contacts where thicker metal and tighter dimensional control requirements preclude the use of lift-off. Particulate problems associated with the etch by-products limit the yield with this technique and have led to a search for alternative contact approaches that can utilize plasma etching.

Photoassisted Etching

A variety of techniques have been developed that make use of light to enhance the etching rate of compound semiconductors. Such approaches have

the appeal that patterning can proceed by direct exposures without a mask. Many different photochemical, photoelectrochemical, and photothermal reactions have been demonstrated in the research laboratory using a variety of lasers and wavelengths. As with photoassisted OMVPE, optical techniques, in principle, permit the creation of specific reactions at the semiconductor surface either by creating reactive species in the gas or liquid phase above the surface or by creating free carriers in the semiconductor. These effects can change the oxidation state of the semiconductor or can change the reaction rate by changing the surface temperature. Most of these approaches are in a research stage, although at least one case--photoelectrochemical etching of lenses on InP-InGaAsP LEDs--has reached advanced development [Ostermayer et al., 1983].

LITHOGRAPHY

Lithography is the process of transferring two-dimensional patterns onto semiconductor chips to permit etching of selected regions of the wafer or to expose selected areas for deposition of metals and dielectrics. Each pattern defines the regions in which the next processing step will be applied, so the patterns must be precisely registered with previous steps. Typically, up to a dozen lithographic steps are involved in the fabrication of an integrated circuit on a compound semiconductor. Achieving higher lateral resolution in the lithographic process is an essential requirement for achieving higher density and faster circuits. Higher-resolution lithography is also the goal of silicon processing technology. Lithographic processes used for fabricating silicon devices generally can be applied directly to compound semiconductor technology. It may be anticipated, therefore, that the research and process development required for future high-speed compound semiconductor circuits will be driven by the demands of the much larger silicon markets. Nevertheless, some of the challenges are briefly discussed here.

Optical Lithography

In current manufacturing processes, lithography is carried out optically by contact or projection printing on thin photosensitive polymeric films spun onto the surface of the semiconductor wafers. The useful resolution of optical lithography today is a little less than 1 micrometer using step-and-repeat technology. Extensions to 0.5-micrometer resolution have been achieved utilizing special multilevel resists and ultraviolet light to reduce diffraction effects. Wafer flatness and surface morphology of compound semiconductor substrates are limitations in obtaining these results. It might be anticipated that ultraviolet lithography using excimer lasers may ultimately achieve 0.25-micrometer features, but for manufacturing this involves considerable development of equipment and photoresist technology. With such fine-line lithography, the depth of focus becomes extremely small, placing stringent requirements

on the optics and wafer flatness. Photoresists that have sufficiently low ultraviolet absorption are required. The throughput of current commercial machines is high, and cassette-to-cassette automated handling is available for compound semiconductors. U.S. companies dominated the manufacture of these systems until 1985, but today Japanese companies have the major market share.

Electron Beam Lithography

Diffraction effects can be substantially eliminated for submicrometer-scale patterns by employing electron beams, x-rays, and ions. Focused electron beams are now the primary writing technology to directly write patterns onto the resist on a wafer with submicrometer resolution. Equipment capable of writing 0.15-micrometer lines is commercially available. Special multilevel resists containing a conductive layer are required because of charging problems encountered with the semi-insulating substrates. The limitation in employing this kind of lithography is the low throughput. This is further aggravated by the complexity of the device design to be written, the resist selectivity, and the high capital cost of the equipment. As a result, electron beam writing is used only where the resolution and alignment demand it, even extending to only parts of a pattern, with the rest being exposed with lower cost optical lithography. Much work is currently being pursued to develop faster and more durable resists, which will increase the productivity of this process. The issue of throughput is much more serious in silicon technology than in compound semiconductor technology, where wafer dimensions and throughput are considerably lower.

Advanced Lithography Systems

Serial electron- and ion-beam lithography (using scanning focused beams) will be used only for relatively low-volume niche applications, such as mask repairing, prototyping circuits, and altering discretionary interconnections. Synchrotron radiation is a source of high-intensity x-radiation adequate (and cost-effective) [Wilson, 1987] for high-throughput lithography.

Masks for x-ray lithography require efficient x-ray absorbing layers deposited on x-ray-transparent membranes. Secondary electron emissions from x-ray absorbers result in an overall background exposure that necessitates the use of high-contrast x-ray resists. On the other hand, masks for projection ion beam lithography must be self-supporting, with openings to pass the ion beams where appropriate. This places severe limitations on mask design.

U.S. manufacturers have a large share of the electron beam mask-making market, and the Japanese dominate the electron beam direct-write market. In the field of x-ray lithography, it appears that the United States has

lost the initiative for the development of commercial equipment to Japan, and possibly also to Europe.

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CHAPTER 8

ION IMPLANTATION AND ACTIVATION

PRINCIPAL RECOMMENDATIONS

Ion implantation is an essential step in the fabrication of most current-generation compound semiconductor integrated circuits. Its importance will increase as focused ion beam technology for selective area implantation matures.

At the present time, however, there is very limited understanding of the ion implantation process in binary or ternary semiconductors. A major yield-limiting factor in GaAs integrated circuits is the wide variation of FET gate threshold voltage over a given wafer and from one wafer to the next. However, it is not possible at present to separate the effects of dopant activation from substrate properties. To meet the performance targets of even current devices, the nature of lattice healing, dopant site selection, annealing history, stoichiometry, and the role of stress associated with capping layers must be fully understood.

To achieve an implantation and activation technology within the next decade that is capable of affordably manufacturing VLSI circuits using GaAs or other compound semiconductors, the following recommendations are presented:

- Develop a fundamental understanding of the thermochemistry of impurity activation and lattice healing following ion implantation. The goal of these studies should be the development of a controllable, reproducible process to achieve uniform dopant profiles and concentrations.

- Encourage exploratory work to evaluate the capabilities, limitations, and unique application of focused ion beam implantation, especially in conjunction with molecular beam epitaxy.

- Develop a reliable, reproducible, low-stress encapsulant for rapid thermal annealing of wafers.

INTRODUCTION

During the past decade, ion implantation has become one of the most important tools of semiconductor fabrication technology. As a technique

for forming doped semiconductor regions, it offers the advantages of simple planar processing, precise control of both lateral and depth distributions of dopants, and the ability to measure the absolute quantity of dopant that has been implanted. Ion implantation is currently used in one or more steps in the fabrication of almost all silicon devices. In silicon technology, ion implantation is a reliable, reproducible, and low-cost processing tool.

The situation is very different for the case of ion implantation into compound semiconductors. Although the process has been used to fabricate GaAs circuits as complex as 16K static RAMs and 16-bit parallel multipliers, and it has also been used to fabricate a variety of devices, including MESFETs, MODFETs, and HBTs, the reproducibility and fundamental understanding of the process are poor. To date, "empirical engineering" of ion implantation has not resulted in a high-yield process for VLSI. It is evident that the affordable manufacture of compound semiconductor integrated circuits will require a greater basic understanding of the ion implantation and activation processes.

ION IMPLANTATION

Ion implantation involves bombarding the semiconductor surface with an energetic beam of ions, derived from a plasma and accelerated to energies typically between 1 keV and 1 MeV. The beam can be magnetically focused for selected area implants, or the sample surface can be masked lithographically to expose only those areas to be implanted. The ions penetrate (typically to about 0.1 micrometer) below the semiconductor surface and rapidly lose their energy by collisions with the semiconductor lattice. The atomic displacements produced by the collisions leave a high density of lattice defects and structural disorder that must be eliminated, or at least greatly reduced, by a thermal annealing step to restore the desired electrical characteristics of the material.

Annealing was conventionally carried out in furnaces, but recently rapid thermal annealing (RTA) with infrared lamps is being used extensively. Laser annealing also has been investigated on a research scale. With the elemental semiconductors silicon and germanium, the annealing process restores the electrical quality of the material, and almost 100 percent of the implanted ions become electrically active donors or acceptors with implant concentrations up to 10^{20} ions/cm^3. In binary or ternary semiconductors such as GaAs, greater atomic rearrangement of the different constituent ions occurs, and a host of problems are created that are not present in elemental semiconductors--e.g., stoichiometry and alloy variation, antisite defects, and amphoteric doping. Furthermore, group III-V compounds tend to decompose nonstoichiometrically during the annealing step. At the high temperature required to heal the damage, the vapor pressure of the group V elements is high (i.e., the vapor pressure of arsenic over GaAs is about 0.1 torr at 1000°C compared with 10^{-7} torr for silicon at this temperature). Thus

annealing must be carried out under a controlled equilibrium pressure of the group V element or by capping the semiconductor surface with a nonreactive dielectric that prevents loss of the group V element.

Peak electron concentrations achieved in GaAs by ion implantation and annealing are typically only in the mid-10^{18} donors/cm^3 region, although 1 to 2 x 10^{19}/cm^3 has been reported occasionally [Gill and Sealy, 1986]. Complete activation of donors in compound semiconductors is achieved only for very low ion concentrations (less than 10^{18}/cm^3). Poor activation results in higher device parasitics and lower carrier mobility than can be achieved with fully activated material. In contrast, p-type dopants can be activated to concentrations greater than 5 x 10^{19}/cm^3. The reason for this behavior is not understood at this time. It is known that the activation level of implanted donors is strongly affected by crystal stoichiometry [Von Neida et al., 1987] and that higher levels of activation can be achieved in GaAs by co-implantation of arsenic ions together with the donors [Krautle, 1981; Park et al., 1981].

It is vital that this issue of implant activation and its variations with process parameters be understood. The variability of the dopant activation from one wafer to the next and even across the diameter of a specific wafer is one of the most serious yield-limiting steps in GaAs IC manufacture. The threshold voltage of GaAs MESFETs can vary by as much as 200 mV across a wafer [G. Troeger, personal communication, 1987] and it is not possible at present to determine whether this is because of the substrate properties, dopant activation, or properties of the gate contacts. For VLSI, a variation of the gate threshold voltage of less than 10 meV is desirable!

IMPLANT ACTIVATION

The introduction of elements by ion implantation leaves the semiconductor far from thermodynamic equilibrium. Restoring equilibrium by thermal annealing requires the shortest possible annealing times to avoid surface decomposition and to avoid extensive diffusion of the implanted ions during the process. Typical implant depths are of the order of 0.1 micrometer. Changes of the implant profile can occur in GaAs even in a few tens of seconds at temperatures of 950°C. Some applications, such as JFETs, require a spatial depth resolution of the implant profile of 2.5 nm, because the precise location of the p-n junction is one determinant of the threshold voltage. No standard approach to implant activation has yet been established. Current efforts seem to concentrate on capped rapid-thermal annealing or capped furnace anneal. In addition, there is continued interest in various arsenic over-pressure techniques, including laying a second wafer over the top of the wafer to be processed.

The United States has led consistently in the development and application of rapid thermal annealing (RTA) for both silicon and group III-V devices. Commercial systems are available from several manufacturers and are widely used both in the United States and in Japan. Reproducible implant activation and profiles place stringent requirements on the encapsulant used for thermal annealing. CVD-deposited SiO_2 and SiN dielectric caps are commonly used in GaAs IC fabrication. However, a problem with these caps is that their thermal expansion coefficients are quite different from that of GaAs. This leads to considerable surface stress, which may induce surface slip in the semiconductor and stress-enhanced diffusion of the implanted impurities. Phosphosilicate glass encapsulants [Singh et al., 1988] have a glass transition temperature below the temperature of RTA and appear to reduce some of these problems. It is essential that, whatever capping technology is used, the cap deposition process be reproducible and the caps adhere reliably. Microcracking or poor adherence of the dielectric will change the stress distribution below the semiconductor surface, with concomitant changes of the impurity profile. Variations of the capping process introduce even more variables that make identification of substrate effects and impurity-activation effects even more difficult.

FOCUSED ION IMPLANTATION

Some of the first serious work on focused ion implantation into compound semiconductors was done in the United States (e.g., Hughes Research Laboratory), but it now seems that the strongest push in this area is coming from Japan. The potential of this technique is particularly promising when combined with molecular beam epitaxy systems [Miyauchi et al., 1986].

Although the doping of compound semiconductors during MBE growth is relatively straightforward, selective area deposition of dopants is not possible in conventional systems. A focused ion beam in the growth system allows selective area doping for specific devices, which can then be followed by further epitaxial growth--without ever removing the wafer from the growth system. This approach eliminates several of the etching and lithography processes that would otherwise be attained only with two-dimensional layer growth.

A further advantage of in situ implantation is that control of <u>absolute</u> dopant concentrations is thus made possible. This is more difficult to achieve in conventional MBE than relative changes of dopant concentrations, especially for dopants whose sticking coefficients are far from unity or are variable with varying growth conditions.

A low-energy implanter coupled with MBE or MOMBE can be used to "count" dopant ions as they are added to the growing layer. Even a low ion energy (e.g., 5 kV) can make the sticking coefficient nearly equal for all dopants. This capability, combined with the ability to implant doping

profiles with lateral dimensional control, makes incorporation of ion implantation in MBE a most versatile tool for precise control of complex device fabrication [Von Neida et al., 1987].

FUTURE POSSIBILITIES

One of the fruitful areas of silicon research in recent years has been silicon-on-insulator (SOI). Recently, several laboratories have demonstrated devices and circuits in which the insulator was formed from a silicon substrate by high-dose ion-implantation or amorphization.

Ion implantation technology for GaAs is in its infancy, whereas for other compound semiconductors it is barely past conception. InP, InGaAs, and AlGaAs have attracted some attention, and other materials such as AlInAs and InAs are now getting "first looks," but it is clear that the understanding of the process and mechanism is, as yet, poor. This is an area where ion implantation research is likely to better serve future device needs. As compound semiconductor technology evolves, other alloys will become integrated with GaAs and silicon technology to combine the advantages of each material system. A generic fundamental understanding of ion implantation in compound semiconductors will advance this capability.

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CHAPTER 9

DIELECTRICS AND METAL CONTACTS FOR GROUP III-V SEMICONDUCTOR

PRINCIPAL RECOMMENDATIONS

The technology used today for electrical contacts and dielectric insulators on compound semiconductor devices was developed many years ago, largely on an empirical basis, with little understanding of the microscopic electronic nature of the semiconductor-film interface. Since these processes did not appear to be yield-limiting steps in the fabrication of first-generation discrete devices or even low levels of integration, there has been little incentive for further development. Recently, however, limitations in the understanding of these interfaces have become evident. This is because device designers are putting more stringent requirements on the reproducibility, uniformity, and reliability of contacts and dielectrics for larger-scale integration of compound semiconductors.

Many workers believe that the currently used Au-Ge-Ni technology for ohmic contacts will not be suitable for multi-chip applications that require bonding in packaged systems. There also is evidence that the W-Si Schottky barrier contact may have problems with yield and variability for LSI applications. New approaches to metallization and dielectric films for encapsulation, passivation, and insulation have emerged at the research level in recent years. A new look at these technologies for manufacture is now appropriate, together with an urgent need for improved understanding of defects at semiconductor interfaces.

There is some evidence that the United States and Europe are currently leaders in the science of the metal-GaAs interface. In metallization technology, Japanese, U.S., and European capabilities are comparable. The W-Si high-temperature gate metallurgy developed in Japan is practiced with state-of-the-art performance in R&D everywhere. Likewise, the Au-Ge-Ni ohmic contact invented in the United States is practiced everywhere with equal performance. The United States generally lags behind Japan in GaAs contact and dielectric manufacturing technology. As indicated elsewhere in this report, this is because of the different commitments of the two nations to developing viable commercial manufacturing technologies.

The United States is now in a good position to take advantage of new developments in contact and dielectric technology. It is recommended that specific emphasis be placed on the following:

- Establish a basic understanding of the origin of Fermi-level pinning in GaAs. Develop reliable procedures for controlling the Fermi-level and defect structure at compound semiconductor interfaces.

- Develop low-interface density and stable high-quality dielectrics for MOS and MIS structures, particularly in InP and InGaAs structures.

- Evaluate the potential of recent innovations in thin film dielectric and metallization procedures for reliable, high-temperature stable LSI fabrication.

INTRODUCTION

Two important challenges facing the commercialization of GaAs and other group III-V materials for VLSI application are the development of reliable, reproducible metal contacts and the development of dielectrics for control and passivation. These challenges confront a common problem. Stated simply, the problem is that at nearly all GaAs-metal or GaAs-dielectric interfaces the Fermi-level is pinned near mid-gap. This causes several major problems in high-speed devices, including high ohmic contact resistance and poorly controlled Schottky barriers, and a lack of surface potential control at the dielectric-GaAs interface. This chapter discusses the interface problem and the state of the art for ohmic and rectifying contacts and dielectrics.

THE INTERFACE PROBLEM

The barrier at most, but not all, metal-III-V semiconductor interfaces is associated with Fermi-level pinning. In GaAs, this pinning occurs about 0.8 eV below the conduction band and creates great difficulty in forming both low-resistance ohmic contacts and rectifying contacts with precisely controlled barriers. The origin of Fermi-level pinning is currently a hotly contested issue. This is because several different observations on n-type and p-type GaAs surfaces cannot be reconciled in a straightforward way. The origin of the defect states responsible for Fermi-level pinning have not been conclusively identified. Several models have, however, been proposed. These are based on defects caused by the deposition processes [Spicer et al., 1980], states associated with surface charge neutrality [Tersoff, 1985], and excess arsenic clusters [Freeouf and Woodall, 1981] on the GaAs surface. Since interfaces also have been observed without pinning [Freeouf and Woodall, 1981; Brillson et al., 1986], variations in the density of anion clusters or native defects seem required by the data rather than intrinsic band structure phenomena [Duke

and Mailhiot, 1985]. The control of unpinned interfaces by any of these techniques could have important implications for future GaAs device manufacture.

Most device technologists agree that, to realize the speed promised by GaAs-based devices in either a monolithic IC or VLSI format, the contact resistance at the source contact must be less than 2 micro-ohm-cm. In addition, the standard deviation in barrier height of the gate electrode must not be more than 10 mV. For an 0.8-eV barrier height, a doping level or a space charge density of about $10^{20}/cm^3$ is needed to produce a tunneling ohmic contact that meets the source contact resistance criterion. This doping level is not easily achieved. A few special reports of high-doping and high-space charge densities are mentioned in the following. Since the maximum practical doping level for GaAs is on the order of about $10^{19}/cm^3$, barrier heights of about 0.5 eV are needed to meet contact resistance requirements. On the other hand, higher gate contact barriers give better performance. Another problem with pinning is that the pinning value is not precisely 0.8 eV. It can vary by 50 to 100 meV from wafer to wafer. Even the workhorse, the W-Si gate contact with its high-temperature stability, can produce an unacceptable spread in barrier height caused by both processing and substrate variables.

As undesirable as the pinning problem is for metal contacts, it has not prevented progress in the high-speed device areas such as MESFETs, HEMTs, and HBTs. It has, however, stymied any progress in the MOSFET area. The reason is simply that pinning at the oxide-GaAs interface leads to a large density of mid-gap traps that terminate the gate voltage and hence prevent modulation of the conductivity in the bulk semiconductor. The correlation of pinning with excess anions has been effective in understanding the differences in the electronic properties of GaAs and InP MOS structures. For GaAs, the equilibrium oxide chemistry predicts the observed excess of elemental arsenic at the interface that has been correlated with a high density of mid-gap states. On the other hand, in InP MOS structures with a low density of mid-gap states, an excess of elemental phosphorous is not observed usually. Fermi-level pinning in InP appears to be less of an issue in MOS devices and passivation than in GaAs. At this time, however, too little effort has been devoted to InP to develop reliable insulators for a manufacturable technology. Furthermore, it is difficult to create sufficiently high Schottky barriers on InP for planar FET devices.

Even though there is not yet universal agreement on the origin of Fermi-level pinning, the research to track its origin has resulted in a recent increase in innovative concepts to form ohmic and Schottky barrier-like contacts and to reduce the trap density in MOS structures. Examples include recent observations of unpinning in air by photochemical [Woodall and Kirchner, 1987] and chemical [Yablonovitch et al., 1987] techniques that remove excess arsenic from GaAs surfaces.

HIGHLIGHTS OF THE CURRENT STATE OF THE ART

Ohmic Contacts: n-type

The Au-Ge-Ni contact is currently the most widely used n-type ohmic contact for GaAs devices and circuits [Braslau, 1981]. Even though the underlying reasons for its ohmic behavior are not understood at this time, it meets the source resistance criteria. The contact was invented in the mid-1960s at IBM for use in Gunn diode studies. It is characterized as an alloyed contact in that it strongly reacts with GaAs at temperatures above 400°C to form a variety of phases that are nonuniformly dispersed at the GaAs interface. The resulting interface is nonplanar. This has led to the theory that the observed proportionality of specific contact resistance to the reciprocal of the doping level is caused by the spreading resistance at protrusions in the nonplanar interface.

Both an advantage and disadvantage of this metallurgy is that it is invasive up to several hundred nanometers from the original interface. This feature is critical to the performance of some current HEMT-type devices, but is thought to be undesirable for other applications, e.g., lasers and bipolar devices. Also, further device processing at temperatures greater than 400 to 500°C causes rapid degradation in contact morphology and a large increase in contact resistance. Another big drawback of Au-Ge-Ni is its lateral dimensional instability upon alloying. It is thought that, as gate lengths and source-to-gate spacing become less than 1 micrometer, this instability will cause both shorting and significant variation in device performance. Perhaps the greatest problem with Au-Ge-Ni is its behavior in lithographic processing. For all practical purposes, subtractive etching of Au-Ge-Ni pattern definition is not feasible using either wet etching or RIE techniques. Ion milling will remove the Au-Ge-Ni, but it is nonselective with respect to GaAs and can cause surface damage. Thus it is considered an unacceptable tool for processing devices. Consequently, most workers agree that the Au-Ge-Ni technology is dead-ended with respect to LSI and VLSI applications.

Rectifying Contacts

Rectifying contacts are needed in circuits primarily for Schottky barrier diodes and as rectifying gate electrodes for MESFET and HEMT devices. As a result of the Fermi-level pinning, the barrier height is nearly independent of the metal used. Therefore, the choice of the metallurgy used for rectifying contacts has evolved around other issues--e.g., stability and etching characteristics. The Au-Ti metallurgy has been used in the past for devices and circuits in which subsequent processing steps did not require temperatures in excess of 300°C.

More recently, technologists have shifted to the W-Si system. This has come about as the result of the need for high-temperature stable

contacts. The newer circuit fabrication methodologies employ self-aligned gate techniques in which the source and drain regions are implanted and annealed at temperatures near 800°C, after the gate metal is deposited. W-Si appears to be stable against this annealing. However, the variation in the threshold voltage of the device, which is controlled by the properties of the gate, is still too large to manufacture LSI circuits of 10K or more gates with an acceptable yield. It is not clear at this time whether this is due to the metallurgy or some other cause. It is clear, however, that any surface strain in the GaAs caused by the metal layers will affect the gate threshold voltage because of piezoelectric effects. It is important to deposit contacts without the introduction of strains and strain variations in the active layer of the semiconductor.

p-Type Contacts

Until recently, little activity has been devoted to p-type contacts because the applications have been limited mainly to discrete optoelectronic devices such as lasers and detectors, where contact resistance demands are less than for high-speed devices. In addition, since the Fermi level is pinned slightly nearer to the valence band and since higher p-type doping than n-type doping can be achieved, it is "easier" to get low contact resistance in p-type material. However, interest in good p-type contacts has been rekindled by the emergence of both high-performance heterojunction bipolar transistors (HBTs) using GaAs and by plans to seriously consider complementary devices and circuits. The current p-type workhorse contact is Au-Zn. Yet this material is thought to be inadequate for LSI circuits using HBTs because of the higher-than-acceptable contact resistance to p-type materials, especially GaAlAs, and poor thermal stability against further high-temperature processing--e.g., rapid and unwanted zinc diffusion.

Contacts to Optoelectronic Devices

Until recently, the contact metallurgies used for GaAs-based discrete optoelectronic devices have been considered adequate. Special care must be exercised to prevent stress and contact migration effects. However, with the drive toward longer-wavelength devices, it is quite likely that new metallurgies will be needed to meet resistance and stability requirements. Since optical links also loom on the immediate horizon, the future needs of the new systems must be addressed now.

Dielectrics for Passivation and Control

The Fermi-level pinning problem discussed earlier limits the role of dielectrics in GaAs devices and circuits to passivation, isolation, and capping layers to prevent decomposition during annealing of ion-implanted structures. The deposition techniques that may be considered "standard"

include both plasma-enhanced chemical vapor deposition (PECVD) for silicon oxides, nitrides, and oxynitrides and both reactive and nonreactive sputtering for materials such as aluminum and silicon nitrides. Organic materials, such as polyimides, also are used as dielectrics for separating multilayered metallurgy. Microwave plasmas are being studied in the laboratory as a potential production tool to produce even better inorganic dielectrics.

Most workers believe that for insulator applications there are no significant problems impeding progress toward manufacturability for the current menu of devices, materials, and processes. However, this is not true for capping layers for thermal activation of ion implantation. It is very difficult to separate MESFET threshold-voltage variations because of the capping effects that occur later--e.g., stress, porosity, and contamination--from those that result from other processing variables, including the starting substrate. Indeed, little effort has been devoted to developing insulators that both minimize stresses (and stress-induced diffusion) at the semiconductor-dielectric interface and improve uniformity of the activated layer. Recent work using phosphosilicate glass caps on GaAs for RTA are reported to produce improved performance. This is because the glass transition temperature of the cap layer lies below the annealing temperature, thereby eliminating stress-induced diffusion, cracking, and slip near the annealing temperature.

Other recent research results are with the use of an epitaxial insulators, either ZnSe [Studemann et al, 1988] or $CaSrF_2$ [Siskos et al, 1984], grown directly on the GaAs surface for MIS devices. The lattice parameter of ZnSe is close to that of GaAs while that of $CaSrF_2$ can be matched to GaAs with the appropriate Sr:Ca ratio. This approach has the potential for producing near-perfect interfaces as well as building the entire MIS device structure in a single epitaxial reactor. To avoid zinc diffusion into the GaAs from ZnSe, a low-temperature deposition process will be required, and subsequent high-temperature processing must be avoided. Finally, until the Fermi-level pinning problem is technologically solved, MOS-type circuits using GaAs will not be part of the device and circuit menus. Yet, InP and GaInAs are possible exceptions. Also, there has been a recent report that (100) GaAs can be unpinned in air using a photochemical technique to produce an arsenic-deficient oxide [Offsey et al., 1986]. It is unlikely, however, that this oxide will be useful for a successful MOSFET technology.

Interface Stability

Thermal stability of the contacts against further processing, including wiring and packaging, is a serious practical problem that device technologists must solve before such applications as VLSI can be manufactured affordably. This is yet another reason that it is highly unlikely that Au-Ge-Ni will be suitable for VLSI--a situation most apparent for circuits requiring insulating layers for multilayered

metallurgy. Most of the currently successful dielectric technologies for insulation require processing temperatures in excess of those that degrade the Au-Ge-Ni contact. In addition, the much higher ion-implantation annealing temperatures not only degrade the Au-Ge-Ni contact but also tend to degrade refractory-metal gate contacts for MESFET devices.

RECENT U.S. RESEARCH

The United States is a leader in innovative concepts for contacts to group III-V semiconductors. This is partially because of an awareness by technologists of the comprehensive surface-science work on III-V surfaces and interfaces of the past decade. The following section is a partial list of U.S. innovation in contacts to GaAs, especially ohmic contacts.

Ge-GaAs Heterojunction Contact

An important lesson learned from interface science and technology is that lattice-matched isoelectronic heterojunctions--e.g., GaAlAs-GaAs--when properly made do not exhibit Fermi-level pinning at the interface [Braslau, 1981]. Indeed, this property has been the reason for the success of many recent high-speed and optoelectronic devices. The Cornell group [Katnani et al., 1984; Stall et al., 1979, 1981; Ballingal et al., 1981; Metze et al., 1980] has successfully applied the lattice-matching concept by developing the Ge-GaAs heterojunction interface to make low-resistance ohmic contacts. The reason for the success is not entirely understood but is due in part to a low-conduction-band discontinuity at the Ge-GaAs interface (reported to range from 0.05 to 0.3 eV), high arsenic doping of the germanium, and a metal-Ge barrier of only 0.5 eV, which appears capable of meeting required contact-resistance criteria. Based on Ge-GaAs phase diagrams, this contact may not be stable above 725°C.

Graded Gap GaInAs-GaAs Contact

It is known that Fermi-level pinning occurs in the conduction band at InAs surfaces that results in an electron-accumulation layer at the metal-to-n-InAs interfaces. This leads to an ideal ohmic contact, since there is no barrier to electron flow. Since Fermi-level pinning produces an 0.8-eV Schottky barrier at metal-to-n-GaAs interfaces, the question is, "Can InAs be used to eliminate this barrier?" The answer is, "Not directly," for at least two reasons [Woodall et al., 1981]. First, it is thought that the bandgap difference between InAs and GaAs is about 60 to 65 percent in the conduction band. This may produce a large band offset and thus would not have any advantage over a metal-GaAs interface. Second, there is a 7 percent lattice constant difference between InAs and GaAs. A heterojunction between the two would contain a large defect density, which is known to cause Fermi-level pinning. However, this

problem has been solved by a continuous grading in composition from GaAs to InAs. This produces a structure with no barrier to electron flow and a measured contact resistance of about 1 micro-ohm/cm^2.

Tin-Doped GaAs by MBE

A barrier height of 0.8 eV requires a doping level of $10^{20}/cm^3$ to produce a tunneling contact resistance of about 1 micro-ohm/cm^2. These values have been approached in layers grown by MBE and doped with tin. A doping level of $6 \times 10^{19}/cm^3$ produces a nonalloyed contact resistance of about 2 micro-ohm/cm^2. A disadvantage of this method is that, for this doping level, there is a surface growth of tin clusters, which produces a rough morphology [Barnes and Cho, 1978; Tsang, 1978; DiLorenzo et al., 1979].

Silicon-Doped GaAs by MBE

It has been found recently [Kirchner et al., 1985] that nonalloyed contacts to MBE-grown GaAs doped with about $10^{20}/cm^3$ silicon atoms have a resistance of about 1×10^{-5} ohm/cm^2. This is a surprising and important result, since the measured bulk electron concentration is only about $5 \times 10^{18}/cm^3$, for which much larger contact resistances are to be expected. Since similar maximum electron densities are obtained for nearly all n-type dopants and crystal-growth methods, many workers have doubted that a low nonalloyed contact resistance could be achieved by high doping. However, surface band-bending has been known for some time to influence dopant incorporation [Schubert et al., 1986; Casey et al., 1971]. Therefore, mid-gap Fermi-level pinning at the surface appears to lead to higher carrier densities than are normally observed in bulk GaAs, which in turn counteracts the high ohmic contact resistance that normally results from the Fermi-level pinning. These results appear to have revived interest in high doping.

p-Type Contacts

The emergence of the heterojunction bipolar transistor (HBT) as a competitive high-speed device has placed new demands on p-type contacts, especially for GaAlAs. Structures that employ p-type GaAlAs for contact purposes are useful in minimizing surface recombination problems in small devices. Unfortunately, Au-Zn on p-GaAlAs produces a high-resistance contact, which in turn degrades device performance. Recently, W-Zn metallurgy has been developed that has greatly reduced contact resistance to p-GaAlAs [Tiwari, 1987].

Theory of Contact Resistance

Until recently there has been little work on the theory of contact resistance at metal-GaAs interfaces that have a finite Schottky barrier height. Previous work [Chang et al., 1971] has been most important and has the benefit of agreeing closely with experiment. However, the work makes assumptions that are known to be wrong, which has led to attempts to improve the theory [Boudville and McGill, 1985]. Recent theories have the unfortunate feature of predicting far lower resistances than are actually obtained.

New Approaches to Rectifying Contacts

It is important to note the innovative work being done in the United States on Schottky barrier modification and multilayer majority-carrier rectifiers. There is work at Stanford University, the University of Illinois, and Cornell University both on modifying the effective barrier height through near-surface-layer doping and on planar doped barriers, in which the rectification properties are controlled by doping and layer thickness using MBE. AT&T Bell Laboratories studied a similar structure using compositionally graded layers of GaAlAs. The Japanese strategy in this area seems to be a combination of trial and error, variations of current schemes, and adaptive engineering. In this vein, they have recently reported the use of LaB_6 as a promising high-temperature-stable Schottky barrier material for GaAs MESFET devices.

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CHAPTER 10

SPECIAL CONSIDERATIONS FOR GROUP II-VI COMPOUND SEMICONDUCTORS

PRINCIPAL RECOMMENDATIONS

Materials and processing technologies for II-VI compound semiconductors are much less advanced than those for III-V semiconductors. This is not only because of the absence of a commercial market for these devices (the entire market for long-wavelength devices is currently for the military), but also because the physical and chemical properties of these compounds make them much more difficult to prepare and process than III-V compounds. Currently, the uniformity and reproducibility of material composition and quality are poor and the price is high.

New approaches to the growth of mercury-containing II-VI compounds are currently under development using MBE and MOCVD techniques that have been developed for III-V compound semiconductors. These approaches offer the potential for a breakthrough for the fabrication of II-VI devices both on lattice-matched II-VI substrates and on lattice-mismatched GaAs and silicon substrates. Without a breakthrough, it is doubtful that the projected performance advantages of second-generation systems will be achieved at the longer wavelengths. If reliable devices can be made with high yield and low cost, a considerable potential commercial market exists for II-VI semiconductor devices. Commercial possibilities also exist for wide-gap and magnetic II-VI semiconductors, as well as for longer-wavelength mercury-containing compounds. To develop the potential of this materials system, the following recommendations are presented:

- Develop low-temperature growth and processing techniques for large-area wafers and abrupt interfaces. Explore more fully the potential of photon-assisted and plasma-assisted growth and alternate organometallic sources for low-temperature MOCVD and chemical beam epitaxy.

- Develop an improved substrate technology for low-defect-density lattice-matched substrates (CdMnTe, CdZnTe) in parallel with alternate lattice-mismatched substrates.

- Explore the integration of II-VI materials and devices with III-V and group IV technology.

- Study effects of defect formation and dopant incorporation in II-VI materials at lower growth temperatures.

- Develop procedures for reliable p-n junction fabrication.

INTRODUCTION

The II-VI semiconductor systems offer a wide range of material parameters for optoelectronic applications. Optical energy gaps range from about 3.7 eV, in the blue for zinc sulfide, to 0 eV gap, in the semimetals HgTe and HgSe. Ternary and quaternary semiconductors can be fabricated with band gaps throughout the wavelength range. The electro-optic coefficients are, in most cases, larger than those of III-V semiconductors in the equivalent wavelength range. By adding magnetic ions, manganese in particular, to the semiconductor composition, it is possible to induce very large magneto-optic effects near the semiconductor band edge. With moderate magnetic fields, Faraday rotation comparable to that in the best ferromagnetic insulators (i.e., YIG) can be achieved for applications such as optical isolators.

Despite the great potential of II-VI semiconductors, significant development efforts have been devoted only to HgCdTe for infrared detection and, to a much lesser extent, ZnS for short-wavelength visible display applications. Consequently, this chapter deals almost exclusively with HgCdTe processing issues for infrared detection applications. It is important to emphasize, however, that progress in developing this materials system will have an impact in a much broader context. The integration of II-VI and III-V materials is already in progress in the research laboratory. For instance, wide-gap II-VI insulators can be grown epitaxially on GaAs. Narrow-gap HgCdTe with GaAs buffer layers has been grown on silicon substrates.

Optimistically, it can be anticipated that the traditional problems associated with II-VI semiconductors will be considerably reduced or overcome with new approaches to materials processing. When this occurs, a wide variety of novel device structures will be feasible throughout the entire wavelength range offered by II-VI semiconductors.

While many of the processing issues are generically similar to those of III-V materials, problems associated with substrate growth and epitaxy are generally magnified in II-VI compounds. In this chapter, the discussion highlights the specific differences encountered with the processing of HgCdTe and its constitutents HgTe and CdTe, compared with the issues in III-V materials and devices discussed earlier in this report.

HgCdTe has become critical to DOD and NASA for application to infrared systems. Photoconductive detectors are currently in production and form

the baseline for infrared technology. However, extensive efforts are under way to develop photovoltaic array technologies for the next generation of higher-performance systems. HgCdTe has such flexibility that it has become almost a universal material for IR detection. It is a complex material requiring extraordinary care and understanding in its preparation and handling; however, costs are coming down because of increased production, increased experience in the industry, and increased competition.

Infrared detectors are experiencing an annual growth rate of 29 percent in delivered quantities [The Aerospace Infrared Detector, Market, 1984]. Projected requirements by 1993 for infrared detector focal plane arrays will be about 44,000 units per year for the tactical market, primarily for HgCdTe. Strategic requirements for midwave (MWIR) and shortwave (SWIR) arrays will substantially increase this demand as space-borne surveillance systems become operational. Commercial applications for infrared detectors are also increasing in areas such as process monitoring, surveillance, and inspection, but the total volume in these areas is small compared with the military markets.

Emerging materials that are under investigation as potential infrared detector materials are dilute magnetic semiconductors, other II-VI alloys such as HgZnTe and HgMnTe, and layered materials based on group IV superlattice type structures. Work on these materials is at an early stage of development, and it is premature to judge their merits.

HgCdTe DEVICE ISSUES

Device Structures

It is generally agreed that the current photovoltaic device technologies based on homojunctions in HgCdTe will not be adequate for second-generation focal planes, especially for cut-off wavelengths greater than about 10 micrometers. Work on heterojunction devices has increased dramatically, and considerable success has been achieved in demonstrating the potential for these devices. In addition, basic studies of these heterostructures are under way to optimize performance [Migliorato and White, 1983; Bratt and Casselman, 1985].

Current HgCdTe heterojunctions are mostly graded-gap structures produced by the interdiffusion of the mercury and cadmium during growth. Typical widths of the graded regions are 0.4 to 3.0 micrometers, depending on the growth method. Barriers to minority-carrier transport can be formed in the graded-gap structure by optimizing on the location of the p-n junction, the width of the junction depletion layer, and the material properties on both sides of the junction.

Superlattices in HgCdTe have been proposed as new composite materials that offer significant advantages over conventional alloys for application to infrared devices [Smith et al., 1983]. The band gaps, and therefore the cut-off wavelengths, will likely be easier to control than those of the alloys at long wavelengths. The wavelength response of the alloy has a singularity near the HgTe end of the composition range. This makes composition control an extremely difficult, if not impossible, problem as the wavelength increases beyond 12 micrometers. First, no such singularity occurs in the superlattice structure, since the band gap is controlled by the thickness of the HgTe and CdTe layers. Second, the leakage currents in devices made in small-gap materials increase with decreasing bandgap and with decreasing effective mass in these materials, i.e., the smaller the gap, the smaller the effective mass. In superlattice structures, the relationship between band gap and effective mass is decoupled to some extent and thus have the potential of improving device performance.

Device and Material Requirements

The rapidly evolving device concepts and designs for second-generation focal plane arrays have created a situation where no universal agreement exists on the precise material parameters that will be required. There is agreement that producibility will not be achieved without larger supplies of large-area, high-quality material to permit progress on the learning curve in process development. Material uniformities of 0.002 mole fraction CdTe, typical in 1-in. wafers today, will have to be matched, at least, in wafers of 3 in. or larger. Specific parameters, such as doping density and type, configuration, and lifetime, are dependent on the particular approach. Experience from the III-V area indicates that control of the electrical, metallurgical, and interface properties also will be required in the II-VI materials. [A summary of the material technology in HgCdTe can be found in National Materials Advisory Board, 1982].

Interdiffusion of the HgTe and CdTe looms as one of the potential limitations to fabricating HgTe-CdTe superlattices and heterojunction devices. Present understanding of the interdiffusion is insufficient to allow accurate predictions on the limitations. Efforts to reduce the interdiffusion through the use of low-temperature growth techniques currently is receiving substantial attention and will require a significant breakthrough before they are entirely successful.

Doping in superlattice structures remains an issue. Questions about the types of defects normally occurring in these structures and the role of impurity atoms require resolution. Transport properties across heterojunctions and normal to the superlattice layers are sensitive to the band offsets and scattering mechanisms, all of which require extensive understanding. The predicted advantages of junction leakage and array uniformity of superlattice structures require confirmation.

Finally, device designs based on superlattices have not been adequately engineered. Specific device designs and the processing sequences need definition and implementation.

SUBSTRATE TECHNOLOGY

CdTe Substrates

Critical to the future success of HgCdTe as a detector material is the development of a suitable substrate for large-area epitaxial growth. The substrate should be lattice-matched with HgCdTe over a large range of compositions, have a suitable thermal expansion coefficient, be chemically compatible with the constituents at the growth temperature, and be available in sufficient size and purity. In addition, the application to IR detection requires that the substrate be transparent to IR to allow for back-side illuminated arrays.

The growth of bulk HgCdTe substrates has historically presented special problems because of the mercury in the crystal and because of the separation of phase boundaries in the alloy. At typical growth temperatures of about 850°C, mercury vapor pressures of tens of atmospheres exist in the growth ampoules, with the constant threat of explosion and safety hazard. Crystals are currently in production using a variety of bulk techniques in sizes ranging from 0.8 to 1.5 cm in diameter. The crystals have composition gradients both radially and axially that require extensive characterization and selective sawing to minimize these gradients in processed wafers. The wafers are seldom single crystal across their entire area and usually have low-angle grain boundary substructure. In spite of these problems, this material has been the standard production material for photoconductive array manufacture.

The materials now used most extensively for substrates are CdTe and the alloy CdZnTe. CdTe has a 0.4 percent lattice-mismatch with HgTe, but it satisfies the requirements of chemical compatibility, thermal expansion, and IR transparency. CdZnTe can be lattice-matched with the entire range of HgCdTe alloy compositions, but the additional constituent introduces complications in achieving a uniform composition (and lattice constant) during substrate growth. Both materials are particularly difficult to grow in large single-crystal form because of a very low energy for defect and twin formation and because the low thermal conductivity at the melting point leads to poor thermal profiles for crystal growth from the melt.

The status of commercially available substrates is shown in Table 10.1. In general, the material continues to be limited in quality and in size, with the predominant concerns being the low-angle grain boundaries and high dislocation densities. These defects result in corresponding imperfections and poor morphology in epitaxial layers grown on the

TABLE 10.1 Status Substrates for Epitaxy[1]

Material	Sources	Cost	Quality: DCRC/FWHM[2] (arc seconds)	Quality: EPD[3]	Precipitates	Structure
CdTe						
Vert. Bridgman	II-VI Inc. Eagle Pitcher Fermionics Cominco Nippon Mining	$80-140/cm^2 Additional premium for areas > 1 in^2 (6.45 cm^2)	16-40	(1-10) x 10^5/cm^2	Variable to boule size to 10 mm dia. Density up to 10^8/cm^3 Occasional boule with no precipitates > 1 μm diameter	Cellular Low-angle grain boundaries "Micro" twins Boules have high density of twins
Horiz. Bridgman	G.S.M.[4]	$80/cm^2	11-15	(1-10) x 10^4/cm^2	No data	No low-angle grains Fewer micro twins
CdZnTe						
Vert. Bridgman	II-VI Inc. Fermionics	$80/cm^2	17-35	(1-10) x 10^5cm^2	Similar to CdTe in density Precipitates are needle-like	Cellular Low-angle grain boundaries Fewer twins in boules
CdTe/Sapphire						
OMVPE	Eagle Pitcher	$80/cm^2	approx. 200	No information available	Not observed	No data

1. Purchase specifications for substrates that can be met by various suppliers
2. DCRD = double cyrstal rocking curve
   FWHM = full width half maximum
3. EPD = etch pit density
4. G.S.M. = GalTech Semiconductor Materials

substrates. There is no indication that captive (in-house) producers of these materials have achieved a breakthrough in material quality relative to the commercial suppliers.

Thick epitaxial layers grown on CdTe by LPE have been reported to be indistinguishable from those grown on lattice-matched CdZnTe. Lattice mismatch effects are observed at the growth interface, but interdiffusion of the HgCdTe-CdTe boundary leads to a graded region with a reduction of strain away from the interface and no increase in the dislocation densitites in the layers. Indeed, II-VI compounds appear to be quite "forgiving" in terms of their defect structure when grown on lattice-mismatched substrates.

Alternate Substrates

Because of the difficulty in growing large-area, high-quality CdTe substrates, recent efforts have been focused on growth on alternative substrates that are more robust and are available in larger wafer sizes. Primary efforts have been aimed at sapphire for MWIR applications and GaAs for more general application out to longer wavelengths. Growth on GaAs substrates offers the potential for monolithic integration of III-V and II-VI devices.

In most instances, binary CdTe is grown as a buffer layer onto sapphire or GaAs by a vapor-phase deposition process followed by an epitaxial layer of ternary HgCdTe by LPE or VPE. CdTe on sapphire is commercially available in 2-in.-diameter wafers. LPE growth of HgCdTe has been reported on these substrates with quality comparable to that produced on bulk CdTe. The use of GaAs as a substrate has received much attention for vapor-phase epitaxy of HgCdTe despite the large (about 14 percent) lattice mismatch between GaAs and CdTe. However, 2-in. wafers with good CdTe surface morphology and uniform thickness and transparency have reportedly been grown by MOCVD [Anderson, 1986]. Likewise, MBE-growth of CdTe on GaAs has demonstrated the viability of this approach. By use of MBE and MOCVD, both (100)- and (111)-oriented CdTe can be grown on GaAs, depending on the initial surface preparation and growth conditions [Feldman and Austin, 1986]. The morphology of (111)-grown material is superior to that of (100), but the highest-mobility HgTe has been grown on (100)-grown CdTe buffer layers.

An anticipated problem with the large lattice mismatch of CdTe on GaAs is the interface dislocation structure that can propagate through the epitaxial layer. This defect structure has an effect on the diffusion of gallium and arsenic across the interface, especially during higher-temperature growth. Under some conditions, the mismatch appears to be accommodated near the growing interface, and significant "healing" of the material occurs in thicker CdTe buffer layers. At this time there is insufficient evidence to determine whether the performance and yield of

devices grown on these layers are comparable to those on conventional bulk CdTe substrates.

EPITAXIAL GROWTH

Epitaxial growth techniques have been in development since the late 1970s and have been reviewed elsewhere [National Materials Advisory Board, 1982]. The primary growth process currently in practice is LPE, but extensive efforts are under way to develop both MOCVD and MBE. These techniques are emphasized in the discussion that follows.

Liquid Phase Epitaxy

LPE techniques have made tremendous advances in recent years and are satisfying a critical short-term need for compositionally uniform device-quality material. Composition uniformities and repeatability of 0.002 mole fraction CdTe in $Cd_xHg_{1-x}Te$ for $0.2 < x < 0.4$ are routinely achievable.

Growth of HgCdTe from tellurium-rich solutions is being used by a majority of laboratories. Techniques include open-tube sliders with controlled mercury overpressure, and dipping or tipping methods in pressurized growth vessels. Growth from mercury-rich solutions has not been pursued as extensively as tellurium-rich growth because of the mercury containment problem near 400°C. Large mercury melts of 5 kg or greater are required to minimize composition gradients throughout the layer thickness and to obtain adequate reproducibility. However, higher-purity material can be produced by this procedure, and doping with indium donors and arsenic or antimony acceptors is straightforward.

The major limitations in continued advancements in LPE are the lack of suitable large-area substrates (typical substrates currently range from 6 cm^2 to 15 cm^2 in area), the prohibitive substrate cost, and the interfacial composition gradation from about 0.4 to 3 micrometers from the rapid interdiffusion of the constituents at the growth temperature. These problems will severely restrict the application of LPE for second-generation photovoltaic devices and more advanced multilayer and heterojunction devices that require abrupt interfaces.

Vapor-Phase Epitaxy

Apart from the economic advantages offered by the vapor phase techniques recognized earlier in the III-V materials, there are some fundamental advantages that are critical to future advancements in HgCdTe device technology. First, the substrate and deposited layer need not be thermodynamically compatible, as is necessary in LPE. This factor is the major driver in the development of alternate substrates. Second, the

reduced growth temperature that is possible with VPE leads to the inherent reduction of defects and reduced interdiffusion of the constituents. These abrupt interfaces are necessary to achieve the required device performance. At the outset, it must be emphasized that, while vapor-phase technologies are emerging as very promising for the growth of future device structures, none has yet been developed as a process for large-scale manufacture.

Metallo-organic Chemical Vapor Deposition

Two approaches are currently being investigated for achieving uniform growth of HgCdTe at a sufficiently low temperature to maintain an abrupt interface. One is pyrolysis with either precracked compounds or with compounds thermally less stable than conventionally used in MOCVD. The other is ultraviolet photolysis of the compounds.

Conventional pyrolytic growth of binary CdTe and HgTe has been successful in the 350°C to 420°C temperature range using conventional dimethyl- and diethyl-compounds with elemental mercury. Growth of these materials has been reported on CdTe, CdZnTe, and a variety of alternate substrates such as GaAs and InSb. No fundamental problem appears to exist in the growth of either of these consitutents when done independently. Growth rates in excess of 10 micrometers/hour have been reported regularly, and the uniformity of growth is limited only by the reactor design.

Conventional pyrolytic growth of the ternary alloys has presented tremendous problems. The growth conditions for the constituents are almost mutually exclusive and depend critically on the microscopic temperature and flow distribution on the substrate as well as the specifics of the reactor design. Composition gradients across the wafer are typically 10 mole percent/cm, and growth rates are typically less than 1 micrometer/hour. The reasons for a strong inhibiting effect in the growth rate when both constituents are present have not been identified.

The search for less stable organometallic compounds of tellurium has led to the use of di-N-propyltelluride (DNPT), di-isopropyltelluride (DIPT), and ditertiarybutyltelluride (DTBT). Growth of HgTe and CdTe has been reported at 220°C with these materials [Hoke and Lemonias, 1986], but no progress was reported in achieving low-temperature growth of HgCdTe. The use of precracking of the constituents has been reported with some success at 225°C [Lu et al., 1986].

The growth of alternating HgTe and CdTe layers and relying on the rapid interdiffusion of the constituents for homogenization (the interdiffused multilayer process, IMP) has been quite successful at growth temperatures around 400°C. Growth rates are acceptably high with this process, and uniformities of the layers are now approaching that of LPE (near 0.002 mole percent CdTe over a 1 cm^2 area).

Growth temperatures can be reduced by using ultraviolet photolysis to break the metal-carbon bonds nonthermally. Results have been reported on HgCdTe growth at temperatures between 200°C and 300°C using either high-pressure mercury lamps or high-intensity lasers. Growth rates are currently very low, and no assessment of the quality of the material grown by this technique has been reported. Interface widths of about 40 nm have been reported.

The photoassisted technique has great potential as a low-temperature growth process for the alloy. An understanding of the photolytic reaction process is essential before progress can be made in establishing a practical process. Improvements in reactor design also are essential to prevent photolytic decomposition at the windows and to produce the required uniform illumination.

The critical areas for development of MOCVD are the chemical processes involved, the reactor design, and sources for alkyls. Increased emphasis on an understanding of the gas-phase reactions occurring in MOCVD must occur. This understanding will have to incorporate the effects of less-stable alkyls and the dissociation and nucleation processes involved in growth. Sources of optimum compounds must be developed, and this involves both price and purity considerations. Current limitations in the doping of layers is often attributed to purity problems with the alkyls.

The design of the reactor is of critical importance to achieving large-area uniform growth. Growth kinetics are very dependent on local flow conditions, and therefore, as mentioned in Chapter 6, a detailed understanding of the flow dynamics in reactors is essential.

Molecular Beam Epitaxy Growth

The growth of HgCdTe and other mercury-based films and multilayers by MBE presents special problems because of the high vapor pressure and small sticking coefficient of mercury. Special provisions are required in the equipment design for mercury pumping and cryoshrouding to prevent re-evaporation of mercury from the chamber and to control the chamber ambient atmosphere. The low growth temperatures and the slow, controlled growth make MBE attractive for the synthesis of layered structures such as heterojunctions, quantum-well structures, and superlattices. A number of researchers have demonstrated growth of HgCdTe, CdTe, and HgTe at temperatures in the 150°C to 200°C range and interface widths of less than 10 nm [Harris et al., 1986; Faurie et al., 1986; Noreika et al., 1986]. Data on layer properties remain sparse, but some data on both n-type and p-type layers have been reported. Electrical properties are extremely sensitive to growth conditions at the low growth temperatures. Layers grown in the 150°C to 185°C range contain inhomogenous strains and a variety of two-dimensional structural defects. The growth of layers has focused on the use of GaAs substrates with CdTe buffer layers.

Doping of the layers is reported to be relatively easy, and the growth of HgZnTe and HgMnTe is possible with MBE. Selective dopant incorporation using photoassisted deposition techniques in MBE appears to be a promising approach to controlling the electrical characteristics of layers. There is interest in HgZnTe and HgMnTe as alternatives to HgCdTe for IR detectors. Since theory shows that cadmium destabilizes the weak Hg-Te bond, both zinc and manganese are currently being investigated as replacements for the cadmium.

The vapor-phase epitaxial techniques appear to be the only way to produce device structures suitable for future-generation infrared devices. Two critical areas must be supported for this development to occur and currently are the overriding limitations to a producible device technology:

- Development of low-temperature epitaxial technology for HgCdTe, either MOCVD or MBE, to achieve the goals of large-area wafers with abrupt interfaces.

- Development of a lower-cost, large-area substrate for epitaxial growth of HgCdTe. Improvements in the crystal growth of CdZnTe should not be ruled out in favor of the alternate substrates but should be carried on in parallel until the applicability of alternates has been proved.

DEVICE PROCESSING

The critical feature sizes required for MCT devices for infrared detector applications are well within the capabilities of the equipment available for semiconductor processing. The major problem encountered stems from the automated nature of current equipment suitable for GaAs and silicon. The nonstandard and nonuniform size and shape of II-VI materials available today cannot be handled in automated equipment without major equipment modification. As a result, HgCdTe technology is not benefiting from equipment and processing advances being developed in GaAs and silicon, but HgCdTe requires custom equipment with a low level of automation and a high skill level for operators. Establishing a material technology compatible with GaAs technology advances is essential for these materials to be cost-effective in the future.

Junction Formation

Currently there is no universally accepted technique in the industry for junction formation. The advantages of ion implantation seen in GaAs have not been realized in HgCdTe. Implantation generally produces n+ layers due to implant damage, regardless of the implanted species. Control of lateral and depth positioning of the junction region, expected of ion implantation, is not achieved. Understanding and control of ion implantation is empirical at this time, and understanding of the complex

nature of the atomic processes involved is lacking. Ion implantation has been used successfully to fabricate detectors in HgCdTe in the 3- to 5-micrometer range, but this is not a highly regarded technique for long-wavelength devices.

Efforts are directed toward in situ doping during growth and diffusion processes for junction formation. Techniques are proprietary, and an accurate assessment of the producibility of these technologies is premature. Both approaches have demonstrated excellent device performance, but both are immature processes and need further development.

Surface Passivation Technology

The II-VI compounds, HgCdTe specifically, do not suffer from the same fundamental surface-passivation limitation encountered in GaAs. MIS devices with low surface-state densities are being produced as an alternative to p-n junction photovoltaics for infrared detection. Native oxides and low-temperature deposited SiO_2 have been used with varying degrees of success to passivate the HgCdTe surface. The understanding of the surface chemistry and surface interactions involved is rudimentary. Results appear to be very nonreproducible, and specific processing details are very proprietary in the industry. Recently, sulfurization of the surface has been reported as a possible alternative to oxidation [Nemirovsky et al., 1986]. Surface-state densities are reported to be low and more controllable than with oxidation. Although no fundamental limitation is apparent in passivating HgCdTe, there is no process sufficiently under control and sufficiently understood to make the transition to manufacturing for photovoltaic or MIS arrays.

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CHAPTER 11

PROCESS CONTROL AND GROWTH-PROCESSING-DEVICE INTERACTIONS

PRINCIPAL RECOMMENDATIONS

Knowledge of the influence of materials on device performance is woefully inadequate. At present, cause-and-effect relationships are obscured by a vast number of process-related factors and a poor understanding of the interrelationships between material properties, process parameters, and device yield and performance. It is not yet clear how even such obvious and easily characterized materials properties as impurities and dislocations affect eventual device behavior. With the low volumes associated with compound semiconductor manufacturing and the large number of process variables, the required understanding will be difficult to achieve through statistical yield alone. Such understanding will require coordinated studies of each process. These should be performed with test structures specifically designed to detect or even amplify the effects of controlled material-properties variations on device performance and yield. The DARPA-established pilot lines offer an opportune vehicle to couple such studies.

New diagnostic capabilities are required to effectively monitor the various processes and to evaluate materials. Diagnostic capabilities should be included in the design of manufacturing equipment. Advanced systems could operate on information gained from in-process diagnostics to provide intelligent automatic control of sophisticated process lines. To this end the following recommendations are presented:

- Establish coordinated experimental programs designed to determine the relationships between materials properties, process parameters, and device performance.

- Initiate research efforts to develop materials screening and in-process diagnostic procedures.

- Enhance exchange of materials and processing information such as uniform test procedures, materials standards, and safety procedures, e.g., through topical workshops.

- Develop new NDE technologies for the control of the materials moving through the production line.

INTRODUCTION

With increasing levels of integration, the yields of complex monolithic circuits become increasingly sensitive to materials properties. A "killer" defect that would result in the loss of one device out of hundreds on a wafer patterned with discrete devices could eliminate an entire circuit out of a small number of circuits on an LSI wafer [Stapper et al., 1983]. Thus the yield is reduced by a factor comparable to the level of integration. It therefore becomes increasingly critical to identify materials and inhomogeneities that result in unacceptable device performance and yield at the earliest possible stages of device fabrication. It is necessary to inspect wafers at frequent steps during device processing and to establish the acceptable range of process parameters to maximize yield. Because of the large number of processing steps, each of which typically has a large number of variable parameters, process control becomes extremely complex and involves sizable complex computer-controlled data-acquisition systems for statistical analysis.

The information obtained from the analysis of an established process can eventually be used to develop accurate numerical simulation to model the process. At the present time, however, insufficient reliable data are available to allow accurate process simulations for GaAs. The development of the required data base is hampered by the low volume of GaAs integrated circuit production and the lack of well-established processes. Little information is therefore available on the relationship between the materials and process parameters and the eventual device performance and yield.

INGOT AND WAFER QUALIFICATION

Before processing, wafers are inspected for mechanical properties such as flatness, surface polish, and dimensions. These characteristics have, in general, been standardized and are easily understood by both wafer vendors and users.

Ingot qualification proceeds by processing selected wafers from an ingot being evaluated, along with wafers from a previously qualified ingot. In one pilot line, for instance, every 21st wafer from an ingot is evaluated. After ion-implantation and thermal processing, a variety of parameters are measured, such as implant activation (resistivity) and substrate isolation. If the data fall within previously established specifications, the ingot is accepted. If not, the remainder of the ingot is sent back to the vendor, exchanged for a different one, and the process is repeated. Since each device line has different procedures and criteria for ingot qualification, it is not generally possible for the substrate vendor to guarantee ingots prior to shipment. Indeed, it is not possible even to guarantee that two ingots grown under apparently identical conditions will exhibit the same performance during qualification.

While improvements in the consistency of GaAs substrates will eventually make such a qualification unnecessary, it is essential that an understanding be established of how the substrate and process variables (such as deep-level defect densities, mobility, carrier density, stoichiometry, dislocation density, and subsurface damage) relate to material and device parameters following processing. Optical imaging, x-ray, and electrical techniques are available for wafer-scale characterization of these properties. A study of the threshold voltage of FETs patterned over an entire wafer (FET microscopy) can be used to study device behavior. Yet none of these have been applied for rapid routine wafer evaluation.

Background of Silicon Technology

Many of the process monitoring, control, and in situ diagnostics issues in compound semiconductor processing are the same as those found in the manufacture of VLSI silicon circuits a decade ago. Techniques, such as visual, mechanical, optical, and electrical tests on special test wafers, used to evaluate and account for the calibration, uniformity, and quality of the process steps have been readily adapted to GaAs. The properties of test chips located at several sites on completed wafers are measured, recorded, and tracked and designed to evaluate special steps. These tests allow the process and equipment to be monitored for the uniformity achieved across wafers and reproducibility throughout wafer lots. The test circuits can be used for the characterization of line width, line-width uniformity, lithography alignment accuracy, wafer distortion during processing, and other defects.

In addition to the common checks used in Si-VLSI processing (such as resistance measurements on test wafers or on special test structures on device wafers to check ion implantation dose uniformity, annealing temperature cycles, and film deposition equipment), it is necessary to conduct more detailed checks on GaAs processing because different GaAs substrates often give different implant profiles, even when processed under identical conditions. Thus, in compound semiconductor processing, considerable effort is spent in qualifying ingots to obtain reliable and reproducible results.

In-Process Diagnostics

Basic understanding of the behavior of materials under various processing conditions can, to a large extent, be achieved in research laboratories or in pilot lines specifically designed for process development. In these circumstances, in situ diagnostics permit real-time monitoring and control of process variables. It is most important, however, that the information derived from such basic studies be related to the eventual performance of the materials in a device line. This requires close coordination of fundamental research and device development

activities. A good example of the poor understanding of materials-device relationships is the lack of consensus as to whether dislocations in GaAs substrates affect the behavior of FETs fabricated on the substrates. Japanese workers have presented convincing evidence of the variation of FET threshold voltage with proximity to a dislocation. Other researchers find equally convincing evidence to the contrary.

It is apparent that results obtained in different laboratories using different starting materials are obscured by complex interrelationships between different process parameters. This emphasizes the need for controlled experiments with confirmation in different laboratories. It is clear that in situ diagnostics of key parameters will be desirable in production lines. MBE machines typically have considerable in situ diagnostics that allow growth rate monitoring, RHEED monitoring of the growing surface, and Auger studies of composition. In MOCVD, little in situ diagnostic capability is typically available in commercial machines.

Individual researchers have incorporated optical (luminescence, Raman) techniques for monitoring reactant species near the substrate surface [Karlicek et al., 1983], mass spectrometers to analyze gases in the OMVPE growth chamber [Ban, 1971; Jen et al., 1987], real-time measurement of the growth rate with a microbalance [Shaw, 1970; Lee et al., 1987], or holographic techniques for observation of gas flows [Giling, 1982]. Similarly, in situ plasma diagnostics in plasma etching and deposition systems may result in improved reliability and uniformity. Equipment manufacturers should consider incorporating some diagnostics in production machines, as, for instance, in Czochralski growth, where attempts are being made to monitor the solid liquid growth interface and the thermal profile of the growth environment to obtain better control of the parameters of substrate wafers.

At the present time, most of these activities are isolated projects that address only specific steps of semiconductor processing. Clearly, only selected diagnostic techniques will be incorporated in a manufacturing environment, but until manufacturing processes show high, reproducible yields, much more effort must be placed on coordinated understanding of materials-processing-device relationships.

Non-Destructive Evaluation

In addition to in-process diagnostics, non-destructive evaluation (NDE) procedures are required for proper quality control. Such techniques should be rapid, contactless, and usable under ambient conditions. Procedures are constantly evolving, even in silicon technology, for use in production environments. For compound semiconductors, there is a critical need for the development of such new technology. Examples include techniques for contactless substrate wafer evaluation (e.g., EPD, resistivity, flatness); methods to evaluate the uniformity in composition and thickness of epitaxial layers; methods for measuring linewidth

uniformity across wafers; and methods for measuring wafer strain. Indeed, at each step, NDE prevents the added cost of processing inadequate wafers through the entire device line. Such evaluation procedures contribute greatly to the overall development of process control.

CONCLUSION

Examination of the history of silicon IC manufacturing development provides useful guidance for compound semiconductor development. For instance, as silicon ICs approached VLSI densities, the cost of preventing inadvertent contamination during processing increased rapidly. After careful studies based on statistically significant samplings, it was shown that impurity gettering, as interstitially formed oxide precipitates within the wafer, could improve process yields. This caused a shift from the purest, most perfect substrates to the use of wafers with controlled defects. It is likely that similar improvements will be obtained in the processing of compound semiconductor ICs. An attempt to evaluate the effects of defect control cannot be successful without a much greater understanding of the entire process. Without appropriate diagnostics and screening procedures, incremental improvements in device performance and yield will come slowly and at great expense. Organizations that gain a firm understanding of process control will be in a position to capitalize with superior yields. At present, Japanese companies place more emphasis than U.S. companies on substrate evaluation, process modeling, and manufacturing techniques. This understanding will serve as a base for wider applications of compound semiconductor technology.

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CHAPTER 12

PROCESS AND ENVIRONMENT

PRINCIPAL RECOMMENDATIONS

Minimizing particle contamination of wafers during all steps of semiconductor processing is critical to high-yield production of semiconductor devices. Thus, the following are recommended:

- Process equipment and clean rooms must be developed that minimize the generation of particles as well as the deposition of particles on wafer surfaces. The insulating nature of GaAs substrates may make the problem significantly greater than equivalent silicon processing facilities.

- Techniques must be developed for monitoring contamination by particles of dimensions less than 0.1 micrometer.

- An understanding of the small (0.01 to 1.0 micrometer) particle deposition process in the complex geometrical environments used in processing must be obtained by theoretical modeling of fluid flows as well as by experimental modeling with well-characterized aerosols. Studies should include the effects of electrostatic charge with a view to electrostatic control of particle velocity.

PROCESS ENVIRONMENT

During all stages of semiconductor processing and device fabrication, a clean environment is essential. The deposition of microscopic particles onto the wafer surface at any stage of processing is a serious yield-limiting factor in large-scale integrated-circuit fabrication. It is obvious that larger particles (greater than 0.1 micrometer) on the wafer surface directly interfere with fine-line lithography and thin-film deposition processes, particularly as feature sizes continue to shrink. Even smaller corrosive particles (0.01 to 0.1 micrometer) derived from combustion of fossil fuels can seriously reduce device lifetime because of the effects of electrochemical corrosion during device operation. These particles may be embedded beneath dielectrics or encapsulants. While these issues are important for all semiconductor fabrication, and problems become more severe as device dimensions are reduced, they are particularly important in compound semiconductor technology because the delicate wafer surface does not permit effective cleaning and removal of particles from

contaminated surfaces. The high resistivity of semi-insulating compound semiconductors exacerbates the problem because of electrostatic effects.

At the present time, an understanding of the control of filtration processes, particle deposition velocities, and particle size distributions in various processing environments is very limited. Extensive research and development activity is currently under way in Japan, where the effort appears to be far more organized than in the United States. A well-organized proposal to produce a "super-fine environment," involving university, industry, and government, is currently under way in Japan. A maximum deposition rate goal of 0.001 particles/cm^2/hour for particles greater than 0.25 micrometer is anticipated by industry.

The need for research in understanding particle-deposition processes extends to complex geometries and environments within crystal growth and film deposition equipment, as well as in laminar flow hoods and clean rooms. Current analytical techniques to measure particle sizes in the 0.01- to 1-micrometer range and size distributions include laser scattering systems (i.e., Doppler velocimetry for airborne particles), ultraviolet laser scattering (developed by Hitachi), and automated SEM (for deposited particles). An important result of experiments performed to date is that the particle deposition velocity changes very rapidly with particle size, the minimum value occurring for particle sizes of a few tenths of a micrometer. For larger particle sizes, gravitational effects become increasingly important, whereas for smaller particles the diffusion rate increases rapidly. Thus, as semiconductor manufacturing enters the submicrometer-scale era and critical particle sizes drop below 0.2 micrometer, the effects of the higher deposition velocities of small particles will become an increasingly serious problem. Measurements of airborne particle distributions alone do not provide a sufficient measure of the seriousness of fine particle contamination of semiconductor wafers.

GLOSSARY
(Terms found in this report)

Note: Chemical formulas are not included in this listing.

APD - avalanche photodiode
CBE - chemical beam epitaxy
CSBH - crescent-substrate-buried heterostructure
DARPA - Defense Advanced Research Projects Agency
DFB - distributed feedback

ESCA - electron spectroscopy for chemical analysis
FET - field effect transistor
GSMBE - gas-source molecular beam epitaxy
HB - horizontal Bridgman (crystal growth)
HBT - heterojunction bipolar transistor

HEMT - high electron mobility transistor
IC - integrated circuit
IR - infrared (area of the electromagnetic spectrum)
JFET - junction field effect transistor
LEC - liquid encapsulated Czochralski (crystal growth)

LED - light emitting diode
LPE - liquid phase epitaxy
LSI - large scale integration
MBE - molecular beam epitaxy
MCT - mercury cadmium telluride (HgCdTe)

MESFET - metal-semiconductor field effect transistor
MISFET - metal-insulator-semiconductor field effect transistor
MIS - metal-insulator-semiconductor
MITI - Ministry of International Trade and Industry (Japan)
MOCVD - metallo-organic chemical vapor deposition

MODFET - modulation-doped field effect transistor
MOS - metal-oxide-semiconductor
MOSFET - metal-oxide-semiconductor field effect transistor
MWIR - midwave infrared (area of the electromagnetic spectrum)
MOMBE - metallo-organic molecular beam epitaxy

NTT - Nippon Telephone and Telegraph Company
OMVPE - organometallic vapor phase epitaxy
PBT - permeable base transistor
PECVD - plasma-enhanced chemical vapor deposition
PIN - positive-intrinsic-negative (diode)

RAM - random access memory
RHEED - reflection high energy electron diffraction
RF - radio frequency
RTA - rapid thermal annealing
SAM - separate absorption and multiplication (photodiode)

SDHT - selectively doped heterostructure transistor
SIMS - secondary ion mass spectroscopy
SMSB - Strategic Missile Support Base
SOI - silicon-on-insulator
SWIR - shortwave infrared (area of the electromagnetic spectrum)

UHV - ultrahigh vacuum
VB - vertical Bridgman (crystal growth)
VLSI - very large scale integration
VPE - vapor phase epitaxy
YIG - yttrium iron garnet

APPENDIX

BIOGRAPHICAL SKETCHES OF COMMITTEE MEMBERS

ALASTAIR M. GLASS received a B.S. degree in physics from the University College of the University of London in 1961 and a Ph.D. degree in solid-state physics from the University of British Columbia in 1964. He was AERE research fellow at Kings College of the University of London from 1965 to 1967. In 1967 he joined AT&T Bell Laboratories, moving through various technical and managerial positions to his present position as head of the Optical Materials Research Department. He served as U.S. representative on the International Advisory Committee on Ferroelectrics since 1979 and was chairman from 1981-1985. He was chairman of the Optical Materials Subcommittee of the Conference on Lasers and Electro-Optics in 1985 and 1986. He has participated as a member or chairman of numerous technical and government conferences and working groups and as editor of a number of technical publications. He is a member of the Institute of Electrical and Electronic Engineers. In 1987 he was elected to the National Academy of Engineering. His areas of expertise include bulk crystal growth of III-V and II-VI materials, epitaxial growth of compound semiconductors by LPE, MBE, and MOCVD, semiconductor materials characterization and processing, and novel IR transmission materials.

JULIAN G. BLAKE received a B.A. degree in physics from Amherst College in 1966 and M.A.T. and Ph.D. degrees in applied physics from Harvard University in 1969 and 1973, respectively. He was lecturer in physics at Harvard from 1973 to 1981 and served as director of the Gordan McKay Laboratory's Division of Engineering and Applied Physics at Harvard from 1975-1981. At Exxon Solar Power Company he managed process development from 1981-1984. In 1984 he joined Eaton Corporation, where he is now chief scientist of Thin Film Systems. He is a member of the American Association of Physics Teachers, Society of Photo-Optical Instrumentation Engineers (SPIE), and the American Society of Metals. His areas of expertise include photoelectron counting statistics, optical properties of amorphous silicon and germanium, and thin film deposition and characterization equipment development and improvement.

ROBERT A. BURMEISTER received a B.S. degree from the University of Wisconsin in 1961 an M.S. and Ph.D. degrees in 1962 and 1965 from Stanford University in materials science. He worked as assistant in materials research at Stanford University from 1961 to 1965. In 1963 he had a concurrent position as member of the technical staff at Bell

Telephone Laboratories. He joined Hewlett-Packard Laboratories in 1965, where he is now head of the Materials Research Department. He is a member of the American Physical Society and the American Institute of Mining, Metallurgical, and Petroleum Engineers. His areas of expertise include preparation and growth of compound semiconductors and magnetic materials, measurement of optical and electrical transport properties, and physical property measurement.

PETER P. CHOW received a B.A. degree in chemistry from the University of Wisconsin in 1968 and a Ph.D. degree in physics from the University of Minnesota in 1977. He worked as principal research scientist at Honeywell Systems and Research Center from 1977 to 1985. In 1985 he joined the Physical Electronics Division of Perkin Elmer Inc. as manager of MBE Research and Development. He is a member of the American Physical Society, American Vacuum Society, and Society of Photo-Optical Instrumentation Engineers. His areas of research include semiconductor crystal growth, device physics, IR materials, vacuum technology and equipment development, and optical materials.

LESTER F. EASTMAN received a B.E.E. degree in 1953, an M.S. degree in 1955, and a Ph.D. degree in 1957, all in electrical engineering from Cornell University. He remained at Cornell University as instructor in 1954 and moved up to professor of electrical engineering in 1966 and to the John L. Given Foundation Professorship in 1985. He has served as consultant in electronics for numerous industrial companies. He was visiting associate professor of electronics at Chalmers Technological Institute (Sweden) in 1960. He was a visiting member of the technical staff at RCA Research Laboratories in 1964 and a visiting member of the technical staff at IBM in 1985. He has been a member of the DOD Advisory Group on Electron Devices since 1978. In 1986, he was elected to the National Academy of Engineering. He is a fellow of the Institute of Electrical and Electronics Engineers. His areas of expertise include semiconductor materials, physical electronics, and electronic devices, especially in microwave frequencies.

HARRY C. GATOS received a diploma degree in inorganic chemistry from the National University of Athens in 1945, an A.M. degree from Indiana University in 1948, and Ph.D. degree from the Massachusetts Institute of Technology in metallurgy in 1950. He served as instructor in inorganic chemistry at the National University of Athens from 1942 to 1946 and as research associate and member of the research staff at Massachusetts Institute of Technology from 1948 to 1952. From 1952 to 1955, he worked as research engineer at E. I. duPont de Nemours & Co. At the M.I.T. Lincoln Laboratory, he served as leader of the chemistry and metallurgy group from 1955 to 1959 and as associate head and head of the Solid State Division from 1959 to 1962. As an MIT faculty member he served as professor of metallurgy and molecular engineering from 1962 to 1966, and he has been professor of electronic materials and molecular engineering since 1966. He is a member of the American

Chemical Society, the Electrochemical Society, American Physical Society, American Institute of Mining, Metallurgical and Petroleum Engineers, and American Academy of Arts and Sciences. In 1983 he was elected to the National Academy of Engineering. His areas of expertise include electrochemistry, electronic materials, crystal growth, semiconductors, and applications.

JAMES S. HARRIS, JR., received a B.S. degree in 1964, an M.S. degree in 1965, and a Ph.D. degree in 1969 from Stanford University, all in electrical engineering. He worked at the Rockwell International Science Center from 1969 to 1982 as a member of the technical staff, manager of GaAs, and director of optoelectronics research, respectively. He joined the faculty of Stanford University in 1982 as professor of electrical engineering and became director of the Solid State Laboratory in 1984. He is a senior member and fellow of the Institute of Electrical and Electronics Engineers, American Physical Society, and the Electrochemical Society. His areas of expertise include semiconductor device physics, electro-optical devices, solar cells, photodiodes, lasers, epitaxial growth of III-V compounds, and ion implantation.

HARVEY C. NATHANSON received a B.S. degree in 1958, an M.S. degree in 1959, and a Ph.D. degree in 1962 from Carnegie-Mellon University, all in electrical engineering. He was instructor in electrical engineering at Carnegie-Mellon in 1959. He joined Westinghouse Electric Corporation in 1962, where he moved through various technical and managerial positions to his current position of Manager of Microelectronic Devices in the Microelectronic Devices Department of the Solid State R&D Division. He is a member and Fellow of the Institute of Electrical and Electronics Engineers and was president (1978-1979) of the Electron Device Society of IEEE. He was a member of the DOD Advisory Group on Electron Devices (1978-1987) and has chaired and served on various IEEE standardization groups and professional committees. He has numerous patents on semiconductor devices. His areas of expertise include research on IR imaging materials and devices, silicon and GaAs boule growth, charge-coupled devices, microwave materials, circuits and devices, and the VHSIC and MIMIC circuits program.

ELLIOTT PHILOFSKY received a B.S. in metallurgical engineering from Carnegie Institute of Technology in 1963 and an M.S. degree in 1965 and a Ph.D. degree in 1968 from Northwestern University, both in materials science. He worked as research assistant at Republic Steel Research Center and U.S. Steel Research Center in 1961-1962, senior scientist to director of Semiconductor Research Laboratory of Motorola from 1968 to 1978, vice president of technology at AVX Corporation from 1978-1985, and moved to his present position in 1985 as president of Tegal Corporation (Motorola). He is a member of Sigma Xi, American Management Association, American Institute of Mechanical Engineers, American Society for Metals, and International Society for Hybrid

Microelectronics. His areas of expertise include metallurgical processing, semiconductor metalization and assembly, analytical techniques, semiconductor materials research, new process development, and electronic component manufacture.

FRANZ ROSENBERGER received B.S. and M.S. degrees from Stuttgart University in 1964 and a Ph.D. from the University of Utah in 1969, all in physics. He was assistant research professor of physics at the University of Utah from 1970 to 1973, assistant professor from 1973 to 1978, associate professor from 1978 to 1981, and professor from 1981 to 1986. He was also director of the Crystal Growth Laboratory at the University of Utah from 1969 to 1986. In 1986, he moved to the University of Alabama in Huntsville as professor of physics and director of the Center for Microgravity and Materials Research. He is a member of the American Association for Crystal Growth and was chairman of the 1985 Gordon Research Conference on Crystal Growth. His areas of expertise include mass and heat transfer phenomena in crystal growth, interface kinetics, and morphological stability.

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DON W. SHAW received his Ph.D. degree in physical Chemistry from Baylor University in 1965. He joined Texas Instruments, Inc., in 1965 and moved through various technical positions to his present position in 1979 as director of the Materials Science Laboratory. He is a member of the Electrochemical Society, American Association for Crystal Growth, American Chemical Society, and Sigma Xi. His areas of expertise include crystal growth mechanisms, kinetics of vapor phase epitaxial semiconductor growth, materials for solid-state microwave devices, and preparation and properties of GaAs.

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